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Simulation study of Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET for high temperature applications

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ABSTRACT

This paper analyzes the effect of temperature variation on various device architectures i.e. Insulated Shallow Extension Silicon On Nothing (ISESON), ISE and SON MOSFET using ATLAS 3D device simulator for 45 nm gate length. The simulation results obtained with the ATLAS has been validated by comparing it with reported experimental data of SON MOSFET. The simulation results demonstrate that out of three device designs, the ISESON MOSFET is the most suitable device for high speed, low voltage and high temperature applications. The integration of ISE and SON onto the conventional bulk MOSFET leads to the enhancement in analog device performance in terms of device efficiency (g_m/I_{ds}), device gain (g_m/g_d), output resistance (R_{out}) and early voltage (V_{ea}).

1. Introduction

MOSFETs are widely used in amplifiers design, analog ICs, digital CMOS design, power electronics and switching devices for high temperature applications in the area of nuclear power plant and space applications, etc. Therefore, there is practical need for a temperature independent advanced MOSFET architecture that can also reduced the SCEs efficiently. Various impacts of high temperature operations are reduction in threshold voltage, off current (I_{off}) and the drain current due to mobility degradation and increase in intrinsic carrier concentration [1]. At high temperatures lattice scattering dominates that leads to the reduction in carrier mobility.

The silicon on insulator (SOI) architecture have been considered as a potential candidate for CMOS device due to the effective suppression of short channel effects (SCEs) and improved device performance [2]. But the SOI put the physical limits on the channel and buried oxide thickness [3] for sub-100 nm gate lengths. Furthermore, the coupling between the source and drain through the buried layer cannot be decreased when the silicon film thickness of SOI continuously reduces to suppress SCEs. Hence the insulating layer (SiO_2) has been replaced with air having lower dielectric permittivity that can further reduce the junction- and parasitic-capacitance [4]. Due to the lower thermal conductivity of air as compared to SiO_2, enhanced self heating effect is expected as the main potential drawback of SON. In order to further suppress the SCE, caused by the potential coupling between the source and drain through thin buried oxide (air) of SON MOSFET, an additional dielectric pillar [5] (i.e. Insulated Shallow Extension ISE) has been incorporated at the side walls, as shown in Fig. 1, of the channel except at the upper most part i.e. region at which the inversion layer is formed. Due to the presence of additional dielectric pillars at the vertical side walls, the punch-through current path is interrupted which leads to significant improvement in SCEs and reduction of the off current (I_{off}) in ISESON architecture.

The present work investigates the electrical performance (i.e. device gain (g_m/g_d), device efficiency (g_m/I_{ds}), output resistance (R_{out}), early voltage (V_{ea}) and I_{on}/I_{off} ratio) of ISESON MOSFET over a wide temperature range and compared the same with the novel ISE and SON MOSFET using ATLAS 3D device simulator [6]. All device architectures have been optimized for same threshold voltage i.e. V_{th} = 0.25 V @ V_{ds} = 0.5 V by adjusting the metal gate work function.

2. Results and discussions

All the simulations are performed using inversion layer Lombardi CVT model that takes into account the effect of parallel and perpendicular fields along with the doping and temperature dependent mobility models. The quantum effects are not considered in the present analysis since these effects are significant for thickness smaller than 5 nm and for channel length below 10 nm [7].

The simulation results are calibrated with experimental data from bulk SON MOSFET [8], and then incorporating ISE architecture, the analog performance of scaled ISESON is assessed. Fig. 2 shows the comparison between simulated and the experimental

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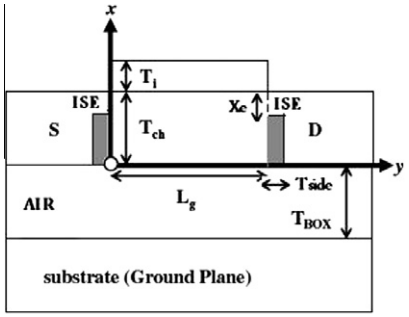

Fig. 1. Schematic cross section view of ISESON MOSFET: L_g is the channel length, T_i is the gate oxide thickness, T_{ch} is the channel thickness, T_{side} is the thickness of side pillars, X_e is the shallow extension depth and T_{box} is the buried oxide thickness.

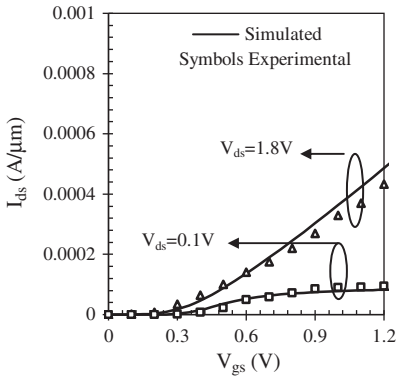

Fig. 2. Experimental and simulated transfer characteristics in linear scale for SON MOSFET with L_g = 80 nm, T_{ch} = 20 nm, T_{BOX} = 20 nm, T_i = 3 nm, T = 300 K.

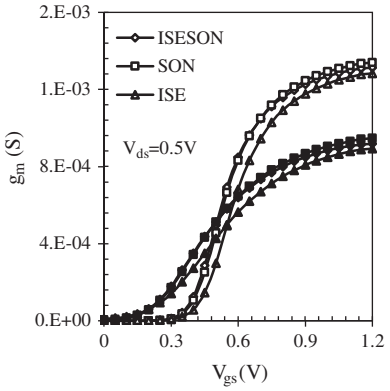

Fig. 3. Simulated variation of trans-conductance for different device architectures under different operating temperatures; solid symbols at T = 500 K, hollow symbols at T = 300 K for L_g = 45 nm, T_i = 2 nm, T_{ch} = 10 nm, T_{box} = 10 nm, X_e = 5 nm, T_{side} = 10 nm, $N_{ch} = 1 \times 10^{17}$ cm^{-3}, $N_{sub} = 1 \times 10^{18}$ cm^{-3}.

results of bulk SON MOSFET under two different drain biases. The good agreement between simulated and the experimental data supports the validity of the simulation results.

In order to compare the various dc characteristics, variation of g_m with V_{gs} has been plotted in Fig. 3 under different operating temperatures. In case of ISE architecture, the dopants from the highly doped S/D region can diffuse at the surface, but beneath the side pillars block them which results in higher effective channel length as compared to bulk MOSFET [5]. Hence the g_m of ISE is lower than the SON MOSFET. Due to the incorporation of ISE structure onto the SON architecture, the effective channel length increases which leads to the reduction in g_m of ISESON as compared to the SON

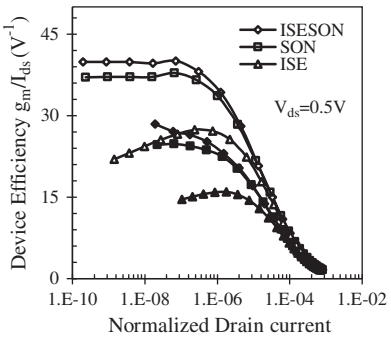

Fig. 4. Simulated results for device efficiency for different devices under consideration for different operating temperatures; solid symbols at T = 500 K, hollow symbols at T = 300 K for L_g = 45 nm, T_i = 2 nm, T_{ch} = 10 nm, T_{box} = 10 nm, X_e = 5 nm, T_{side} = 10 nm, $N_{ch} = 1 \times 10^{17}$ cm^{-3}, $N_{sub} = 1 \times 10^{18}$ cm^{-3}.

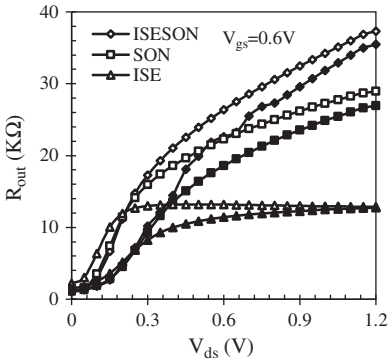

Fig. 5. Simulated variation of output resistance for different architectures at different operating temperatures; solid symbols at T = 500 K, hollow symbols at T = 300 K for L_g = 45 nm, T_i = 2 nm, T_{ch} = 10 nm, T_{box} = 10 nm, X_e = 5 nm, T_{side} = 10 nm, $N_{ch} = 1 \times 10^{17}$ cm^{-3}, $N_{sub} = 1 \times 10^{18}$ cm^{-3}.

MOSFET. Furthermore as the operating temperatures increases, trans-conductance increases below zero temperature coefficient (ZTC) point which leads to leakage current enhancement and thereafter it decreases. However, the percentage reduction in g_m in ISESON is lower in comparison to SON (69%) and ISE (88%) MOSFET.

g_m/I_{ds} ratio is very useful and important design criterion for operational trans-conductance amplifier (OTA). Fig. 4 compares the device efficiency for different devices under consideration for different operating temperatures. The ISESON architectures exhibit higher device efficiency as compared to other configurations over a wide temperature range. Due to lower field penetration from drain to source region, the percentage reduction in device efficiency (with rise in temperature) in ISESON (28%) is lower than the ISE (35%) and SON MOSFET (33%) showing its superior immunity against temperature variation.

Fig. 5 shows the variation of output resistance against V_{ds} for different devices under consideration. An improvement is observed in early voltage for ISESON as compared to ISE and SON MOSFET. In ISESON architecture, coupling path between source and drain has been tremendously suppressed by the buried oxide layer as well as by the side pillars to suppress DIBL and drain conductance leading to R_{out} enhancement. As the operating temperature increases, the reduction in R_{out} with temperature is smaller in ISESON MOSFET (6%) as compared to the SON MOSFET (9%) due to the presence of side pillars. The percentage change in R_{out} in ISE architecture is negligible with operating temperature (at higher V_{ds}) due to the higher effective channel length of the architecture but the magnitude is very small as compared to ISESON architecture even at the room temperature.