



## Quantum simulation study of single halo dual-material gate CNTFETs



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### ABSTRACT

For the first time, a novel single halo dual-material gate carbon nanotube Field-Effect Transistors (CNTFETs) with doped source and drain extensions is proposed and simulated using quantum simulation. The simulations are based on two-dimensional non-equilibrium Green's functions (NEGF) solved self-consistently with Poisson's equations. Comparisons are made for electrical characteristics among four CNTFETs structures, which are conventional single-material-gate CNTFETs (C-CNTFETs), halo single-material-gate CNTFETs (HALO-CNTFETs), dual-material-gate CNTFETs (DMG-CNTFETs), and halo dual-material-gate CNTFETs (HALO-DMG-CNTFETs). The results show that the HALO-DMG structure decreases significantly the leakage current and increases on-off current ratio as well as cutoff frequency. It is also demonstrated that HALO-DMG structure possesses two perceivable steps in potential profile of the channel, which leads to another lateral electric field peak inside the channel, thus improve both carrier efficiency and the immunity against short-channel effects (SCE). Finally, the high-frequency characteristics of the CNTFETs have been discussed based on the channel vertical electric field distributions. The parasitic capacitance has a great influence on the cutoff frequency, and limits the RF performance of the device.

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### 1. Introduction

Carbon nanotubes Field-Effect Transistors (CNTFETs) are promising candidates for fundamental components in the future nano-electronics. Compared to silicon counterparts, due to an exceptionally high mobility, and the near ballistic transport in the channel [1], CNTFETs can obtain higher driving current, faster operation speed and significant reduction in power consumption. These make CNTFETs extremely suitable for high performance CMOS circuit applications. For example, recent progress in CNTFETs has been reported that terahertz cutoff frequency can be achieved with high-frequency and low-noise transistor [2–4].

The major limiting factor for CNTFETs downscaling is the so-called short-channel effects (SCE) which are caused by the increasing charge sharing from the source and drain. To alleviate this problem, different solutions have been proposed to enhance the immunity against SCE [5–8]. Among the possible solutions, dual-material-gate (DMG) structures have been proved to be the most efficient method to overcome the bottleneck of transport efficiency and SCE [9–13]. Due to the discontinuity work function of the gate, this structure leads to potential step along the channel at the conjunction of different gate metals. As the drain potential changes, the step in potential increases, which provides a better shielding of the channel from the drain variation and results in an increase

of average carrier velocity in the channel. Xiang et al. have achieved the preparation of a hetero-gate structure by chemical doping method [14]. Since the gate material may be substantially related to the metal and the oxide, preparation technology of hetero-material gate structure is entirely feasible in practical applications.

On the other hand, halo implantation is generally used to suppress threshold voltage roll-off, drain-induced barrier lowering, and to prevent punch through for CNTFETs, which is another method to increase carrier transport efficiency [15–18]. Besides that, halo structures can also help CNTFETs to achieve the modulation of electric field distributions and electrostatic potential along the channel, thus the devices will have better control of gate over the conductance of the channel.

In order to possess the advantages of both DMG and halo structures which can help reduce SCE and gate capacitance simultaneously, we propose a compound structure called halo dual-material-gate CNTFETs (HALO-DMG-CNTFETs). In this paper, we have investigated the effects of halo for conventional single-material-gate CNTFETs (C-CNTFETs) and DMG-CNTFETs, using two-dimensional numerical simulations, which are based on the self-consistent solution of the two-dimensional Green's functions and Poisson equations. The results show that in the structure we have proposed, SCE are suppressed because of the perceivable steps in the surface potential, which screens the drain potential variation and the cutoff frequency can reach terahertz. However, parasitic capacitance has a great influence on the cutoff frequency, and limits the RF performance of the device.

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## 2. Model and methods

Our model is based on the self-consistent calculation of the potential and charge density in CNTFET [19–24]. The calculation of charge density is using the NEGF. The retarded Green's function of the device is:

$$G(E) = [(E + i\eta^+)I - H_D - \Sigma_D - \Sigma_S]^{-1} \quad (1)$$

where  $\eta^+$  is a positive infinitesimal,  $E$  is energy,  $H_D$  is the Hamiltonian when electrons in CNT is under the best adjacent approximation,  $\Sigma_S$ , and  $\Sigma_D$  is self-energy generated by device's source and drain electrode, which can be solved by calculating the surface Green function using iterative approach. Once we get the Green function, the density of electron and hole in any position in the device can be given by following equations:

$$n(r) = \int_{E_f}^{+\infty} dE [G\Gamma_S G^+ f(E - E_{FS}) + G\Gamma_D G^+ f(E - E_{FD})] \quad (2)$$

$$p(r) = \int_{-\infty}^{E_f} dE \{G\Gamma_S G^+ [1 - f(E - E_{FS})] + G\Gamma_D G^+ [1 - f(E - E_{FD})]\} \quad (3)$$

where  $E$  is partial Fermi level in CNT,  $E_{FD(S)}$  is the Fermi level in drain(source). Then, the carrier densities are put into the Poisson equation of the device and solve it self-consistently. The Poisson equation of the device can be given as:

$$\nabla^2 U(r, z) = -\frac{e}{\epsilon} \rho(r, z) \quad (4)$$

where  $U$  is electrostatic potential,  $\epsilon$  is dielectric constant,  $\rho$  is the distribution of net charge. The Poisson equation is essentially a 2-D problem along the tube ( $z$ -direction) and the radial direction ( $r$ -direction) in cylindrical coordinates, since the potential and charge density are invariant around the nanotube in the coaxially gated CNT transistor.

In the contacts between gate and CNT, the potential  $V$  is determined by Dirichlet boundary condition  $eV = eV_g + \Phi_{CNT} - \Phi_g$ , where  $V_g$  is gate voltage,  $\Phi_{CNT}$  and  $\Phi_g$  is the work function of CNT and gate electrode respectively. The Neumann boundary condition is introduced along the exposed surface of the dielectric, which means the normal component of potential gradient in the boundary is zero to meets the electroneutrality condition.

By using this model, we can get the channel current is:

$$I = \frac{4e}{h} \int dE T(E) [f(E - E_{FS}) - f(E - E_{FD})] \quad (5)$$

In the above equation,  $T[E] = \text{Trace}[\Gamma G \Gamma G^+]$ , which is the transmission coefficient of electron tunneling through the channel,  $E_{FD(S)}$  is the Fermi level of drain(source).

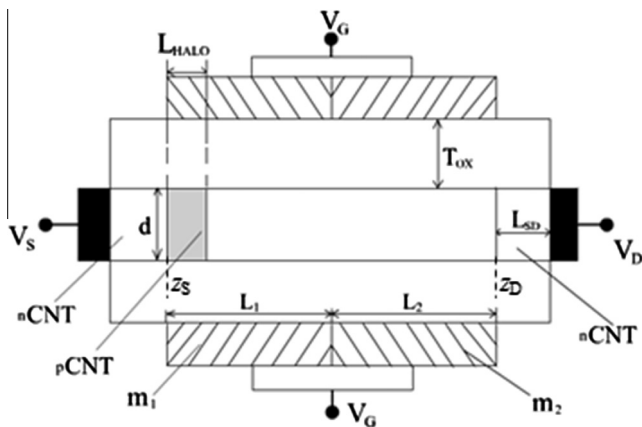


Fig. 1. Schematic cross-sectional view of the proposed CNTFETs.

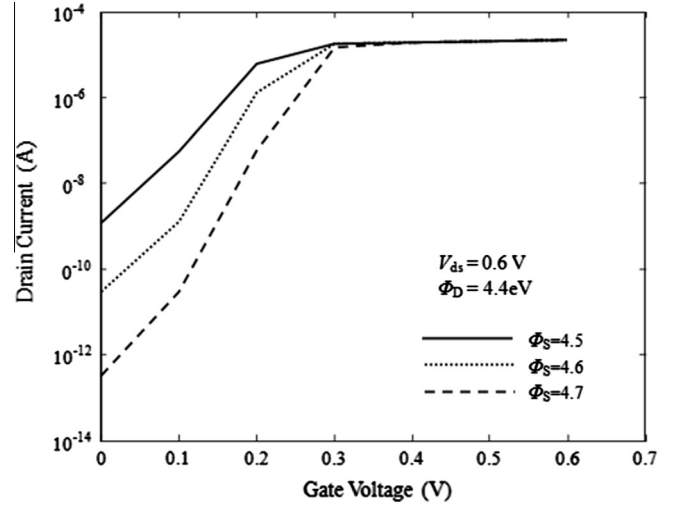


Fig. 2. Transfer characteristics of DMG structure.  $L_g = 20$  nm.

A quasi-static treatment was used to assess high-frequency performance of cntFETs [25]. The intrinsic cutoff frequency of the transistor is computed by

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_g} \quad (6)$$

where the transconductance  $g_m$  and the gate capacitance  $C_g$  are

$$g_m = \left. \frac{\partial I_d}{\partial V_g} \right|_{V_d} \quad (7)$$

$$C_g = \left. \frac{\partial Q_g}{\partial V_g} \right|_{V_d} \quad (8)$$

The total charge  $Q_g$  on the gate can be calculated from the electric flux density at the gate electrode surface

$$Q_g = 2\pi(r_{CNT} + T_{OX}) \int_{z_S}^{z_D} D_r(z) dz + 2\pi \int_{r_{CNT}+T_{OX}}^{r_{CNT}+T_{OX}+t_g} r D_{z_S}(r) dr - 2\pi \int_{r_{CNT}+T_{OX}}^{r_{CNT}+T_{OX}+t_g} r D_{z_D}(r) dr \quad (9)$$

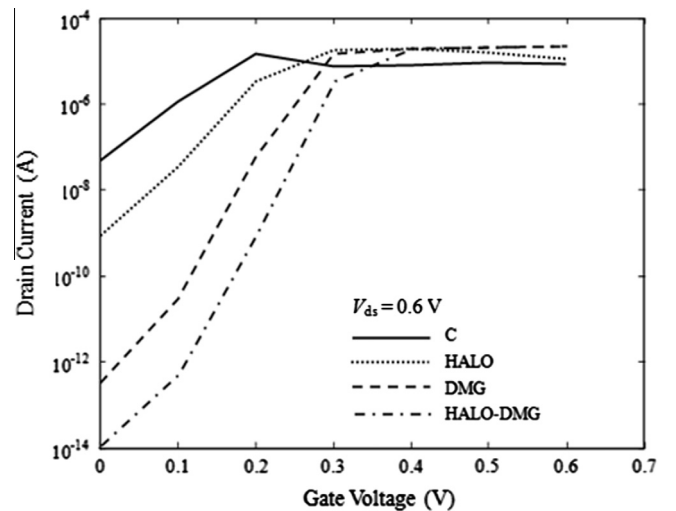


Fig. 3. Comparison of drain current versus gate voltage for C-CNTFETs and DMG-CNTFETs with and without halo doping.  $L_g = 20$  nm.

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