A novel Wireless Network-on-Chip architecture with distributed directories for faster execution and minimal energy

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Wireless Network-on-Chip (WNoC) architectures are introduced to improve performance by reducing the core-to-core communication latency. Conventional WNoCs broadcast messages that increase bandwidth-traffic, communication delay, and power consumption. Studies show that directory-based architectures have potential to address message broadcasting and improve performance. This work proposes a novel WNoC architecture with distributed directories (WNoC-DDs) that supports wireless communications to enhance faster execution by reducing latency. VisualSim software package is used to model and simulate the proposed WNoC-DDs, a WNoC with centralized directory (WNoC-CD), and a traditional 2D mesh by processing different communication scenarios. The proposed architecture helps reduce the total hop count and unwanted broadcasting among nodes in a WNoC-DDs. Experimental results show that the proposed WNoC-DDs reduces communication delay up to 20.54% and 5.40%, respectively, when compared to mesh and WNoC-CD. Similarly, the proposed WNoC-DDs reduces power consumption up to 73.56% and 19.97%, respectively, when compared to mesh and WNoC-CD.

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1. Introduction

The dominant technology such as Network-on-Chip (NoC) is becoming trendy and can solve performance limitations of traditional wired interconnects and productive for System-on-Chip (SoC) architectures. Recent studies indicate that lot of products, such as, processors, cell phones, memory subsystems and many other embedded products are integrated on a single chip and interconnected by NoC [1–3]. The design of multicore systems makes easy to solve complex jobs by working concurrently in parallel with improved execution speed and reduced power consumption [4,5]. Multithreading is a process in which a central processing unit (CPU) can execute several number of threads simultaneously. Memory-balanced scheduling is a thread scheduling approach that improves the performance by balancing memory access requirements but at the cost of interconnects width and bandwidth [6]. However, the programming for large scale multicore architecture is always challenging [7]. The functionality of multicore can be outstanding when the cache coherence is reduced, and it could be less in private memory multicore architectures but are expensive. The shared memory plays a trade-off approach of cost and cache coherence problem. Snooping protocols address coherence issues but are limited to small core counts, whereas

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directory protocols are good for large cores. Recent studies indicate that the snoopy protocols can be extended to 36-core but the power and area are the major drawbacks [8]. The performance and efficiency of communication among cores can be achieved with the implementation of additional parallelism and multithreading.

Multicore designs should assure less chip area, reduced communication latency and reduced power consumption thereby, providing better communication among cores on the chip. NoC architecture, is a technology proposed to overcome the problem of large communication delay among cores in a multicore architecture. Multiple interconnects are proposed to address latency and power issues such as concentrated-sparse mesh [9], millimeter wave wireless interconnects [10], crossbar on-chip interconnects [11]. The primary purpose of those interconnects is to overcome power and latency issues. But the designs are still tough to address performance issues within low cost and scalability. However, with the constraints and limitations of multicore designs, the development of efficient NoC grabbed an outstanding attraction.

The routing paths for efficient communication among cores are different and follow adaptive or non-adaptive algorithms in multicore architectures. In traditional mesh multicasting, the popular non-adaptive technique is XY routing algorithm [12]. Wireless Network-on-Chip with centralized directory (WNoC-CD) architecture [13] uses an adaptive XY routing algorithm to decide the path between nodes [14]. Also, WNoC-CD uses the buffer management to improve the performance by taking care of queuing delays without affecting the throughput rate [15]. The topology of a multicore architecture on chip plays a predominant role in the communication delay. The introduction of directory in multicore architectures, can improve the performance like faster execution and overcome the cache coherence problems [16–18]. However, the centralized directory lacks its performance and slows connections for several reasons such as insufficient bandwidth, increase in network size, and heavy traffic [19].

The existing interconnection technologies such as RF-I and UWB have speed, bandwidth, area, RC (Resistor Capacitor) wired interconnect, and power issues. The proposed distributed directories are Stanford Directory Architecture for Shared (DASH) memory that addresses several issues such as speed problem, bandwidth, traffic, area, power consumption and data sync. In detail, speed problem can be reduced by using XY routing algorithm, bandwidth as well as traffic issues reduced by distributed directories mechanism, area can be narrowed by reducing RC interconnects, and the power is reduced on factors such as selection of shortest path to reach destination. Data sync is better with distributed directories compared to synchronization from individual cores level. In this paper, we propose distributed directories based architecture with wireless routers to overcome centralized directory limitations such as reducing communication delay, hop count, and power consumption.

Section 2 summarizes related published articles. In Section 3, the proposed distributed directories based multicore architecture with wireless routers is introduced. In Section 4, the experimental details are described. In Section 5, experimental results and related discussions are presented. In Section 6, the conclusions of the work are presented.

2. Background study

In this section, we discuss some popular network topologies used in WNoC to reduce the performance bottleneck that may reduce the data throughput, and scalability. We also consider the issues of cache coherence that lead to complication of data exchange between cores, and how a Stanford DASH architecture will address the coherence using customized MESI protocol.

2.1. Popular network topologies

Mostly, the multicore architectures are designed to enhance the performance by utilizing several cores for multiple tasks in parallel. However, the communication between cores is the most influenced consideration to reduce the performance bottlenecks such as latency, power consumption, area, and throughput. The popular interconnect topologies that are employed in NoC architectures are bus, ring, crossbar, and mesh. Photonic integrated NoC overcome the bandwidth barriers in traditional or electronic NoC. In photonic integrated NoC, bus topology has high latency when compared to ring topology for higher loads. Even though the bus topology provides the shortest path, it requires additional transceivers which increases cost and power consumption. Unidirectional ring topology provide better scheduling performance but requires more wavelength and large packet length [20]. Bit error rate is slightly more in bus topology when compared to ring topology. However, the performance of bus and ring topologies is worst for concurrent transmissions of same wavelength that can cause cross talk [21]. Modular decoupled cross bar architecture is efficient for area and power consumption but has power gating, excessive wiring, and performance issues based on workload [22]. Mesh is a popular network topology for multicore architectures that can handle high volume traffic. In a 2D (two-dimensional) mesh network, all cores are connected in a crossbar connection. Mesh topology is introduced in NoC because of its simplicity and scalability. Sparse mesh interconnects are advanced to traditional mesh solving bandwidth and performance issues in high traffic. However, the concentrated-sparse mesh network latency is higher for low traffic workloads [9]. Even though, the mesh has better advantages compared to bus, ring, and crossbar topologies, the issues of bandwidth and inadequate performance yet to be addressed.

Nowadays, the cores are increasing tremendously on a single chip and so it is essential to reduce the wired connects. Wired connects brings several issues such as latency, area, and traffic between the cores. Therefore, the adaption of wireless interconnects plays a crucial role to address the complications of wired interconnects. A complete setup of wireless interconnects is not satisfactory due to bandwidth issues and so the hybrid integration of wired and wireless interconnects typically
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