

3-Dimensional numerical optimization of silicon-based high performance parallel microchannel heat sink with liquid flow

J. Li^a, G.P. Peterson^{b,*}

^a *Department of Mechanical, Aerospace and Nuclear Engineering, Rensselaer Polytechnic Institute, 110 8th Street, Troy, NY 12180, United States*

^b *Department of Mechanical Engineering, University of Colorado, Boulder, CO 80309, United States*

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Abstract

A full 3-dimensional (3D) conjugate heat transfer model has been developed to simulate the heat transfer performance of silicon-based, parallel microchannel heat sinks. A semi-normalized 3-dimensional heat transfer model has been developed, validated and used to optimize the geometric structure of these types of microheat sinks. Under a constant pumping power of 0.05 W for a water-cooled microheat sink, the optimized geometric parameters of the structure as determined by the model were a pitch of 100 μm , a channel width of 60 μm and a channel depth of about 700 μm . The thermal resistance of this optimized microheat sink was calculated for different pumping powers based on the full 3D conjugate heat transfer model and compared with the initial experimental results obtained by Tuckerman and Pease in 1981. This comparison indicated that for a given pumping power, the overall cooling capacity could be enhanced by more than 20% using the optimized spacing and channel dimensions. The overall thermal resistance was 0.068 $^{\circ}\text{C}/\text{W}$ for a pumping power of 2 W.

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1. Introduction

Recent advances in microelectromechanical devices (MEMS), advances in very large-scale integration (VLSI) technologies and the associated microminiaturization of semiconductor devices in general, has led to significant increases in the packaging densities and associated heat fluxes generated within these devices. These increases are typified by the projections in the International Technology Roadmap for Semiconductors (ITRS) [1] that indicates that volumetric heat generation rates will approach $3.3 \times 10^4 \text{ W}/\text{mm}^3$. This level of power generation will require that junction-to-ambient thermal resistances be below 0.14 $^{\circ}\text{C}/\text{W}$ in order to meet the suggested maximum junction temperatures of 85 $^{\circ}\text{C}$ required for long-term, high-performance operation of these devices. One of the

possible methods for removing the resulting high heat fluxes, is to utilize microchannel heat sinks with or without phase change, fabricated as an integral part of the silicon wafers. This approach was first presented over 25 years ago by Tuckerman and Pease [2]. Since that time, numerous investigations have been conducted using a variety of designs and geometric configurations. However, review of the existing experimental results indicates that in the vast majority of these investigations, the geometries evaluated were selected arbitrarily or based upon ease of fabrication, rather than through the use of some sort of theoretical or computational analysis to determine the optimal configuration. As a result, the thermal performance of these non-optimal devices was well below what could be achieved with relatively small changes in the geometry and that the current technology was sufficiently robust to allow the fabrication of these optimized geometries.

While many of the initial investigations were performed on non-optimal geometries, the results clearly indicated a

* Corresponding author. Tel.: +1 303 4928908; fax: +1 303 4928866.
E-mail address: Bud.Peterson@colorado.edu (G.P. Peterson).

Nomenclature

a	thermal diffusivity	\mathbf{V}	vector of velocity
A	total surface area of microchannel	W	width of channel
A_c	area of cross-section of microchannel	W_{pitch}	width of pitch
C_P	specific heat	<i>Greek symbols</i>	
D_h	hydraulic diameter	θ	dimensionless temperature
f	friction factor	δ	thickness of the substrate bottom wall
H	height of channel	λ	conductivity
h	convective heat transfer coefficient	ρ	density
\dot{m}	mass flow rate	μ	dynamic viscosity
N	number of channels	ν	kinetic viscosity
P	pressure	Γ	periphery of the inner wall of channel
\bar{P}	pumping power	<i>Subscripts</i>	
q_w	heat flux	b	bulk liquid
Re	Reynolds number	l	liquid
T	temperature	m	mean value
u	x -direction velocity of liquid	w	substrate
U	dimensionless velocity		
\dot{V}	total volume flow rate		

relationship between the cross-sectional aspect ratio and the flow friction and convective heat transfer for both laminar and turbulent conditions. In a majority of cases, silicon-based MEMS technology was used to create microchannels within silicon wafers that had trapezoidal or triangular cross-sections (anisotropic wet etching on $\langle 100 \rangle$ wafer) or rectangular cross-sections (DRIE or wet etching on $\langle 110 \rangle$ wafers) as opposed to more traditional circular cross-sections. In addition, in most cases, heat was added to the bottom of the wafer, resulting in non-symmetrical heat addition to the channel periphery.

Recently, efforts have been underway to analyze the possible optimal structure for these parallel microchannel heat sinks [3–10]. Among these optimization works, two principle methods were adopted: one is the fin efficiency method [3–6] and the second is a numerical computation method [7–10]. It is interesting to note that optimal geometries suggested by these two approaches were seldom similar. This may be due to the fact that the fin efficiency method requires a number of assumptions, which may vary from one investigator to the next and hence, reduce the accuracy of the results, for example (i) the assumption of the heat transfer coefficient which could vary for different investigations, (ii) the assumption of a constant temperature difference between the solid and the bulk fluid, and (iii) the assumption that the axial heat conduction is negligible. Alternatively, in the majority of the numerical approaches developed, a very simple 2-dimensional heat transfer model was used to determine the optimal value [7,8] or in some cases, a very coarse mesh was adopted [9] for use in the numerical approach. Recently, Li and Peterson [10] proposed a rigorous, 3-dimensional semi-normalized numerical method to explore the optimal geometry of the parallel microchannel heat sinks and demonstrated that

on a silicon wafer with a typical thickness of 450 μm , the configurations first used by Tuckerman and Pease [2] and by Kawano et al. [11], were quite close to the optimized values predicted by the numerical model. Nevertheless, the ultimate optimal geometry was not achieved due to the constraint of the wafer thickness of 450 μm .

In the current investigation, a detailed full 3-dimensional numerical simulation of the conjugate heat transfer problem was conducted in order to analyze the effect of the geometry of these silicon-based microchannel heat sinks on the overall heat transfer performance and to determine the optimal structure of the microheat sink under the assumption of a constant pumping power. The microheat sinks evaluated in this investigation, consist of a 10 mm long and 10 mm wide silicon substrate (1 cm^2). Using this configuration, the effects of the microchannel geometry on the temperature distribution in the heat sink (or the thermal resistance) are investigated. With the optimized geometry, the heat transfer performance of the microchannel heat sink as determined by the variation in the thermal resistance was then calculated for different pumping powers and compared with the existing experimental results. In addition, a number of microfabrication issues are also presented and discussed in terms of the feasibility of fabrication of the resulting optimized, deep trench microchannel heat sinks.

2. 3-D conjugate heat transfer modeling in microheat sinks

Rectangular microchannels can be fabricated using silicon wafers with aspect ratios, H/W , of up to 20:1 using DRIE and 6:1 using KOH wet etching techniques, subject to a number of constraints. These constraints are the result of issues related to the stress and deflection under high

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