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A UNISON framework for analyzing alternative strategies of IC final testing for enhancing overall operational effectiveness

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Abstract

Owing to capacity limit, yield demand, and cycle time reduction, determining proper strategy for the final testing of integrated circuits (IC) device is critical. Since none of the tests can perfectly distinguish good devices from bad, alternative testing strategies consisting of various setups and testing procedures affect the testing results and testing cycle time. However, this problem has seldom been addressed in literature. This study aims to construct a decision framework to analyze alternative testing strategies and thus derive the optimal strategy balancing operational efficiency, cost, and risk. This framework has been implemented in a semiconductor-testing firm in Taiwan. The results demonstrate practical viability of the proposed framework.

Keywords: Decision analysis; IC final test; Semiconductor manufacturing; Operational effectiveness; Manufacturing strategy

1. Introduction

Semiconductor manufacturing is a capital-intensive industry in which on-time delivery, cycle time reduction, fast ramp-up, yield enhancement, and continual cost reduction are the important ways for operational excellence to maintain competitive advantages (Chien and Wu, 2003). The selection of final testing strategies of IC devices is critical in semiconductor companies owing to capacity limit, yield requirement, and cycle time reduction. Because of lengthy wafer fabrication an IC production processes with various sources of variability being involved in the semiconductor supply chains, the final testing of IC devices as the final step in IC production is critical in order to overcome bullwhip effect.

Indeed, an IC-testing strategy is a portfolio (Chien, 2002) of different testing procedures with corresponding setups and recipes. Alternative testing strategies consisting of various tests and setups will affect the sensitivity and specificity of testing results and testing cycle time. On one hand, false-passed products will not only cause customer complaints and product returns, but also impact company reputation. On the other hand, false-failed products will cause loss of IC manufacturer and may also affect normal delivery. In practice, a tradeoff is implicitly made among the decision attributes of cost, quality, and risk to design and

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select testing strategies. However, little research has been done to deal with such decisions systematically and effectively. The difficulty can be traced at least in part to the lack of a decision framework in which the interrelation among the decision elements can be structured and then the involved uncertainty and tradeoff can be analyzed explicitly and systematically.

This study aims to propose a framework for analyzing alternative configurations of testing strategies by considering the tradeoffs among throughput, testing cycle time, and the associated costs and risks to enhance overall operational effectiveness of IC final testing. In particular, the proposed framework integrated statistical decision analysis and cost to model the alternative testing strategies and the involved uncertainties while considering the objectives of increasing testing profit and customer satisfaction. For validation, we conducted an empirical study in a final testing factory of a leading semiconductor company in Taiwan, whose primary products are mask read-only-memory (Mask ROM) and flash memory. The proposed framework can assist the decision makers to design and select testing strategy configuration in light of the condition of testing facility as well as the decision context of semiconductor supply chain.

The rest of this paper is organized as follows. Section 2 presents related studies. Section 3 details the proposed framework. Section 4 describes an empirical case study in a semiconductor final testing factory to validate the proposed framework. Section 5 concludes this study with discussions of the contribution of this study and future research directions.

2. Fundamental

The increasing process complexity for wafer fabrication has caused higher manufacturing costs and longer cycle time. Thus, on-line metrology is set at various steps to inspect the wafer real time, which often causes extra inspection costs and also increases cycle time. Regarding general defect inspection in wafer fabrication, Nurani et al. (1996) defined five parameters of sampling strategy including layers to be monitored, frequency for lots, and number of inspection wafers per lot, percentage area of the wafer and pixel size. Leang and Spanos (1997) proposed a general equipment diagnostic system based on Bayesian theory to assist the operator in finding the causes of decreased machine performance. Chien et al. (2000) developed a framework for optimizing sampling frequency in the light of multiple operational objectives to not only maintain yield level, but also reduce extra cost and cycle time. However, decision analysis of semiconductor final testing strategies has received limited attention.

Bayesian decision discusses the mechanism of using extra new information from appropriate sampling method to update posterior probability and derive expected losses or profits of alternative strategies under uncertainty to select the alternative with the minimal expected loss or maximum profit. There are three basic decision elements in Bayesian decision analysis: parameter space, sample space, and action space. Parameter space Ω is composed of possible states of nature θ_j, i.e., $\Omega = \{\theta_j\}$. Let A denote a set of possible actions, jointly constituting the action space, i.e., $A = \{a_i\}$. Sample space is composed of sampled data. Fig. 1 shows a conceptual framework of Bayesian decision analysis (Sainfort, 1991). When uncertainty involved in decisions and the state of nature θ is not exactly known, prior probability $\pi(\theta_j)$ of θ can be derived based on historical data, expert judgments, or prior ignorance (Chien, 2005b). In addition, data mining can be employed to extract useful information from huge data automatically or semi-automatically collected during fabrication process (Chien et al., 2007). In light of new evidence or additional information provided from sample data x, the

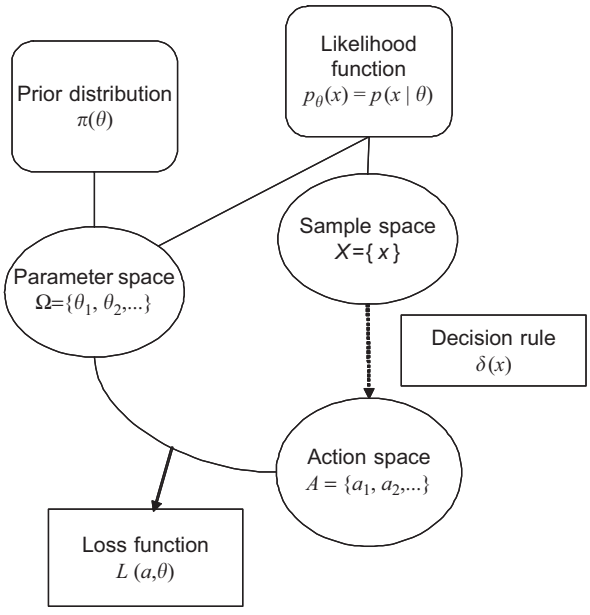

Fig. 1. Bayesian decision analysis (Sainfort, 1991).