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Overall Wafer Effectiveness (OWE): A novel industry standard for semiconductor ecosystem as a whole

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ABSTRACT

As semiconductor industry reached nanotechnology generation and consumer electronics era, the competition is no longer among individual semiconductor companies. Indeed, the collaborations among horizontally specialized value providers are critical for the success of the companies as well as the whole ecosystem. This paper aims to propose a novel index, i.e., Overall Wafer Effectiveness (OWE), to measure wafer productivity and drive various improvement directions for semiconductor ecosystem as a whole. Furthermore, the proposed OWE can be easily extended to incorporate additional attributes such as mask-field-utilization, throughput, and yield for effective management. We conducted a number of case studies in real settings. The results have shown that OWE can be employed as a semiconductor industry standard to drive collaborative efforts among IC designers, equipment vendors, and manufacturers in the ecosystem to enhance total wafer effectiveness. This paper concludes with discussions on value propositions of proposed OWE indices and future research directions.

1. Introduction

The research and application of industrial engineering are facing challenges in light of the changes of industry structures in many countries as well as the evolutionary ecosystems of various businesses. There should be a systematic methodology of "industrial engineering" that focuses on "the industry and ecosystem as a whole" as the subject of study to differentiate industrial engineering from other disciplines. Focusing on semiconductor ecosystem, this paper is part of continuous research efforts to construct a systematic methodology of industrial engineering to investigate the industry as a whole. In particular, semiconductor industry is one of the most complicated industries in which productivity enhancement, yield enhancement, continual cost reduction, fast ramp-up, on-time delivery, and cycle time reduction are the important ways for operational excellence to maintain competitive advantages (Chien & Wu, 2003). Driven by Moore's Law (1965) that the number of transistors fabricated in the same size area will be doubled every 12–24 months to provide more capability at equal or less cost, the semiconductor industry has strived for continuous technology migration and cost reduction. Semiconductor companies have coevolved in the ecosystem (Moore, 1993), in which the companies involved in various layers of semiconductor value chain work cooperatively and competitively to develop new technology, satisfy customer needs, and eventually incorporate the next round of innovations. Therefore, semiconductor industry has a clockspeed (Fine, 2000) faster than other industries for technology migration and thus can provide an important benchmark for other industries.

Semiconductor industry is very capital-intensive, in which the co-evolution of the semiconductor industry has been driven by technical advance and economical interest to maintain the growth and profitability via modularity and virtual integration (Chien and Kuo, 2011). Indeed, corporate manufacturing strategic decisions involve the interrelated elements of the PDCCCR framework (Chien, Chen, & Peng, 2010) including pricing strategies (P), demand forecast and demand fulfillment planning (D), capacity planning and capacity portfolio (C), capital expenditure (C), and cost structure (C), that will affect the overall return (R) of a company, as illustrated in Fig. 1.

In particular, productivity enhancement is critical to improve cost structure for profitability, while conventional approaches focused on miniaturization through technology advances, wafer size enlargement for scale economy, fast yield learning, tool productivity, and supply chain management. To capture the overall equipment performance for identifying and analyzing hidden performance losses, Overall Equipment Effectiveness (OEE) considering equipment availability, utilization, and output quality was developed as

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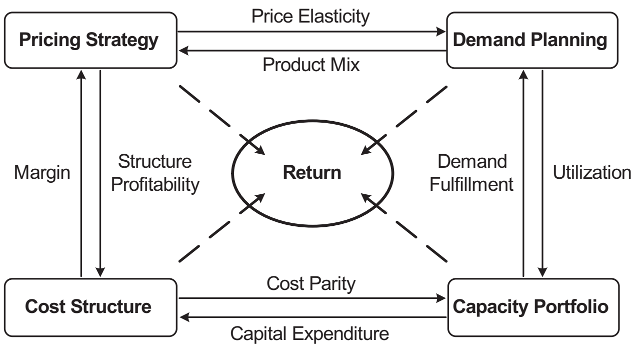

Fig. 1. The PDCCCR framework of manufacturing strategy (Chien et al., 2010).

an industry standard (Nakajima, 1988; SEMI E79-0200, 2000). In particular, SEMI E10-0701 (2000) is the guideline that specifies the definition and measurement of equipment reliability, availability, and maintainability (RAM) for equipment performance based on different equipment statuses for measuring equipment RAM performance, in which equipment time can be decomposed into key blocks associated with the basic statuses and sub-statuses. Furthermore, SEMI E79-0200 (2000) defines OEE as the fraction of total time that equipment is producing effective units at theoretically efficient rates. In particular, effective units denote the number of units processed by the equipment during production time that were of acceptable quality, i.e., actual unit output minus equipment assignable rework and scrap. Nevertheless, conflicts and uncertainties often exist among these performance indices such as cycle time, throughput, WIP (work in process), utilization, and operational efficiency.

OEE indices and SEMI E10 have been widely accepted as a set of industry-wide standards for measurement of equipment productivity among equipment buyers, suppliers, and manufacturers in semiconductor manufacturing. However, there is limitation for evaluating only OEE of a single machine in semiconductor manufacturing. de Ron and Rooda (2005) proposed a new metric to compare and to improve tool productivity by excluding environment factors such as operator, recipe, facilities, material availability, scheduling requirements and used only effective time as the time base. Moreover, Chien, Chen, Wu, and Hu (2007) proposed an Overall tool Group Efficiency (OGE) indices to observe the equipment performance at tool group level and applied statistical efficiency control charts to continuously monitor OEE over time. The equipment performance can be monitored from critical tool groups to single machines via longitudinal analysis and then root-cause analysis of machine statuses can be employed to identify possible performance detractors. In addition, the metrics for OEE is not sufficient to evaluate and track the performance of whole factory. SEMI E124-1107 (2007) defined a set of metrics for overall factory efficiency (OFE) that is the volume efficiency multiplied by the yield efficiency and can be decomposed into the subordinate metrics including the basic metrics as shown in Fig. 2. In particular, the production metrics are used to represent the volume efficiency that considers the performance of throughput rate, cycle time efficiency, and WIP efficiency with respect to the process efficiency. The quality metrics are used to represent yield efficiency that considers the performance of line yield and test yield with respect to the overall material efficiency. The cycle time efficiency and throughput rate efficiency, such as best-case throughput rate and actual throughput rate, can be measured by similar metrics. Thus, the OFE can be employed to evaluate how well a factory is operating compared to how well it could be with the given conditions such as product mix. The metrics of OFE are intended for evaluating the overall efficiency of factory operation, not for diagnosing problems in the factory, though it can be used to indicate whether the factory has poor performance in specific indices such as throughput, utilization, defect density, daily starts and output (SEMI E124-1107, 2007). Alternatively, to diagnose problem and identify bottleneck for improvement in the factory, Muthiah and Huang (2006) proposed the effectiveness metrics of overall equipment effectiveness and Overall Throughput Effectiveness (OTE) for calculating equipment and system productivity for complex-connected manufacturing systems including series, parallel, assembly and expansion subsystems. Furthermore, Kuo, Chien, and Chen (2011) structured the influence relationships of the factors and developed manufacturing intelligence approach to analyze the massive production data and tool data to derive effective rules for cycle time reduction and throughput effectiveness. However, little research has been done to address productivity from the perspective of wafer exposure performance.

To develop a generic methodology to address the wafer productivity for the semiconductor ecosystem as a whole, this paper aims to propose a novel standard, namely Overall Wafer Effectiveness (OWE), for measuring overall wafer exposure effectiveness. OWE can identify different types of wafer area losses owing to equipment, lithography technology, exposure pattern, and production variation. We conducted different case studies to examine the values of proposed OWE. The results showed that the proposed OWE can be used as a semiconductor industry standard and indices to drive collaborative efforts among IC designers, equipment vendors, and manufacturers for enhancing productivity and total wafer effectiveness.

2. Wafer productivity

Most of the existing studies focused on improving operational efficiency such as OEE, cycle time, WIP, and throughput. In particular, since photolithography is generally the bottleneck for wafer fabrication, a number of approaches on scheduling and dispatching (Dabbas & Fowler, 2003; Chien & Chen, 2007), yield enhancement (Allan, Walton, & Holwill, 1992; Cunningham, Spanos, & Voros, 1995; Chien & Hsu, 2006), and tool productivity (Chien, Chen, et al., 2007; Leachman, 1997) in photo area are developed to improve operational efficiency.

This paper proposed a novel approach for wafer productivity enhancement and cost reduction with a set of metrics. The capital investment and operating costs of wafer fabrication are rising significantly because of the increasing complexity of the manufacturing process and the costly fabrication equipment. In order to enhance the competitive advantages for wafer fabrication, it is important to reduce die costs by improving wafer productivity as the technology is keeping migration. The wafer productivity can be defined as the fraction of the effective useful wafer area to the total wafer area.

$$\text{wafer productivity} = \frac{\text{output}}{\text{input}} = \frac{\text{effective useful wafer area}}{\text{total wafer area}} \quad (1)$$

The useful wafer area, the product of number of good die and die size, is determined by yield rate and gross die number. In particular, the problem for determining wafer exposure pattern can be structured as cutting and packing problems or knapsack problems (Chien, Hsu, & Chen, 1999, 2002; Chien, Hsu, & Deng, 2001). Most of the cutting and packing problems are known to be NP-complete. However, this problem can be done within reasonable time limit because of the specific characteristics listed as follows. Firstly, all the cut rectangular pieces of dies and fields from the circular wafer are the same sized. Secondly, the numbers of the dies and fields patterned on a wafer are unconstrained. Thirdly, the dies patterned on a wafer have with equal profit.