Regular paper

Low-voltage subthreshold CMOS current mode circuits: Design and applications

Mohammed A. Eldeeb,⇑ Yehya H. Ghallab, Yehea Ismail, Hassan Elghitani

A R T I C L E  I N F O

Article history:
Received 30 April 2017
Accepted 29 August 2017

Keywords:
CMOS circuits
Current-mode circuits
Gm/Ib design methodology
Low voltage
Self-cascode
Subthreshold

A B S T R A C T

The world has migrated to portable applications ranging from smart phones to Lab on a Chip applications. However, they come with a new set of challenges for analog IC designers. Low voltage operation, small area and low noise are the critical design criteria for portable devices. This paper presents a \( g_{m}/I_b \) based design methodology for low voltage current mode circuits using standard CMOS technology. A second generation current conveyor (CCII) and a current feedback operational amplifier (CFA) are designed using the discussed design procedure. Both circuits operate from a single 0.4 V supply. The CCII is used to implement an instrumentation amplifier. Multiple applications are implemented using the CFA. Post layout simulation using TSMC 90 nm and UMC 130 nm technology show that the presented design procedure is an attractive solution for low voltage CMOS current mode circuits.

1. Introduction

We live in a world that’s constantly on the move. To accommodate, our applications have all become smaller and faster. Starting from laptops and wearable heart monitors to Lab on a Chip applications where multiple labs are integrated onto a single chip a few cm² in area. Fitness trackers for example are rapidly gaining popularity [1]. In sports they are used to enhance the performance of athletes and help them to reduce the risk of injury during training [2]. In medicine, the uses range from glucose level measuring to heart monitoring and automated drug delivery [3]. Physiological signals reside below a few kHz and at most few mV in amplitude [4] which makes them susceptible to flicker noise and external noise sources. These devices require low noise low power miniature analog front-end circuitry. In this paper we present a design procedure for current mode circuits using standard CMOS technology suitable for low voltage applications.

There are various methods for low voltage design [5–7]. The \( g_{m}/I_b \) design methodology has proven to be energy and area efficient when designing operational amplifiers [8,9]. In recent years, interest in current mode circuits has risen primarily due to their ability to operate from a low voltage source [10–16]. Previously published state of the art low voltage second generation current conveyor (CCII) use either bulk driven techniques [17] that occupy large areas due to the required isolation of MOSFETs with different bulk potential. The other technique uses Floating Gate MOSFETs [18] which require extra steps during fabrication. There are few implementations that use Carbon Nanotube (CNT) technology [19]. However, these are not easily integrated into VLSI systems that use standard CMOS technology. In this paper and based on the \( g_{m}/I_b \) methodology, the most commonly used current mode device, [i.e., the Second Generation Current Conveyor (CCII)] is designed, simulated and presented. Then, the CCII is then used to implement a Current Feedback Operational Amplifier (CFA) [20]. A couple of applications using the CCII and CFA are simulated and presented to showcase the feasibility of the design procedure. The remainder of the paper is organized as follows: the behavior of the MOSFET in subthreshold region is discussed in part II. Part III discusses the CCII circuit design procedure, simulation results and applications based on CCII. The CFA circuit design, simulation results and applications based on CFA are presented and discussed in Part IV. Part V concludes the paper.

2. Behavior of MOSFET in subthreshold region

Operating in the subthreshold region with newer technology is feasible as it’s easy to achieve a drain current of few \( \mu \)A which corresponds to a few kHz of bandwidth sufficient for multiple applications like biomedical applications [e.g.: ECG, EEG and EMG]...
(below 1 kHz) and audio applications (20 kHz). The drain current in the subthreshold region is expressed by (1) [8], where the drain current $I_D$ changes exponentially with the gate to source voltage $V_{GS}$. $W/L$ is the aspect ratio of the MOSFET, $V_{TH}$ is the drain to source voltage, $V_T$ is the threshold voltage, $q$ is the electric charge, $k_B$ is Boltzmann constant, $I_m$ and $m$ are process parameters ($1 < m < 2$) and $T$ is the temperature in Kelvin.

$$I_D = \frac{W}{L} I_m e^{\frac{V_{GS} - V_{TH}}{k_B T}} (1 - e^{-\frac{V_{GS}}{k_B T}}) \tag{1}$$

$$V_T = k_B T \frac{q}{q} \tag{2}$$

Fig. 1 shows the drain current $I_D$ plotted against $V_{DS}$ for the NMOS transistor in the TSMC 90 nm technology. For the curve at $V_{DS} \approx 200 \text{ mV}$, the drain current $I_D$ saturates at $V_{DS} \approx 80 \text{ mV}$. Hence the second term in round brackets can be neglected if $V_{DS} \gg 3V_T$ where the MOSFET operates in the saturation region while biased in the weak inversion. Table 1 shows the small signal parameters where the MOSFET operates in the saturation region while biased for a MOSFET in subthreshold with where the empirical coefficient $K$ is dependent on the bias for PMOSFET while constant for NMOSFET. For a MOSFET moves from accumulation to strong inversion, the subthreshold region.

Table 1 shows the small signal parameters for MOSFET in subthreshold saturation region [8].

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$</td>
<td>$I_{D0}/V_{f}$</td>
<td>(3)</td>
</tr>
<tr>
<td>$r_d$</td>
<td>$V_{f}/I_{D0}$</td>
<td>(4)</td>
</tr>
<tr>
<td>$A_0 - g_m/g_d$</td>
<td>$1/I_{D0}$</td>
<td>(5)</td>
</tr>
<tr>
<td>$S_{no}$</td>
<td>$4q(V_{f})^2/I_{D0}$</td>
<td>(6)</td>
</tr>
<tr>
<td>$g_{m1}$</td>
<td>$(K/10)^{1/2}$</td>
<td>(7)</td>
</tr>
</tbody>
</table>

Fig. 2 shows the transconductance efficiency $(g_m/I_D)$ as a MOSFET moves from accumulation to strong inversion. It's apparent that the highest efficiency is achieved in weak inversion, the subthreshold region.

Fig. 3 shows that the gain in subthreshold is determined by the channel length only which is stated by (5). Thus longer channel length will provide better performance. Fig. 4 shows the variation in drain current and transconductance efficiency against channel length. It's noted that the current increases at first up to a certain point and then decreases. The rise in current is attributed to the drop in $V_{TH}$ as channel length increases. The change in $V_{TH}$ becomes negligible after 0.5 $\mu$m and the current decreases as expected from (1) while the transconductance efficiency remains constant for both technologies.

This means that it's possible to increase the gain and bandwidth simultaneously by using a larger channel length. From Eqs. (6) and (7), the increased channel length decreases the flicker and thermal noise.

3. Second generation current conveyor

3.1. Circuit design

$$\begin{bmatrix} i_y \\ i_x \\ i_c \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ v_x \\ v_c \end{bmatrix} \tag{8}$$

Fig. 6 shows the second generation current conveyor (CCII) block diagram. It consists of 2 input ports and 1 output port. Port $Y$ is a high impedance voltage input, port $X$ is a low impedance current input and port $Z$ is a high impedance current output. The CCII can be described using the operational matrix (8). The volt applied at port $Y$ is tracked at port $X$ while the current at port $X$ is tracked at port $Z$. Fig. 7 shows the second generation current conveyor circuit implemented by using an operational amplifier (opamp) in unity gain feedback for ports $X$ and $Y$ with a current mirror stage for port $Z$ [22]. The two stage topology was chosen for its low output impedance, Eq. (10), as the impedance $R_z$ at port $X$, Eq. (11), (ideally zero) is the output impedance of the opamp. Eq. (10), divided by the open loop gain, Eq. (9). Self cascode technique [23] is used to enhance the open loop gain. Fig. 8 shows the procedure for designing a second generation current conveyor using standard CMOS technology in the subthreshold region.

$$A_x = \frac{g_{m1} g_{m9} g_{m10}}{(g_{m1} g_{m9} g_{m10} + g_{m1} g_{m9} g_{m12} + g_{m9} g_{m12})} \tag{9}$$

$$R_x = \frac{1}{g_{d11} + g_{d12}} \tag{10}$$

$$R_c = \frac{g_{m1} g_{m9} g_{m10} + g_{m9} g_{m12}}{g_{m1} g_{m9} g_{m10}} \tag{11}$$

Step 1 – Supply voltage: The differential pair requires 300 mV for the NMOS and PMOS in the first stage to operate as a single MOSFET in saturation. So $V_{DD}$ was set to 0.4 V to achieve the least possible power consumption without affecting performance.

Step 2 – Bias voltage: The biasing was chosen from Fig. 2. A lower biasing voltage would yield higher efficiency at the cost of a much larger sizing to drive the required current.

Step 3 – Transistor length: As low impedance is required at port $X$, the channel length supplying maximum current was chosen for MOSFETs M9-10 and M13-14. As for the input stage, the channel length was set to 1 $\mu$m and 2 $\mu$m to achieve the required open loop gain without causing a significant drop in drain current.

Step 4 – Second stage transistor width: By analyzing Fig. 5, it's apparent that the optimum channel width for the second stage is around 20 $\mu$m for the TSMC design and 10 $\mu$m for the UMC.
دریافت فوری متن کامل مقاله

امکان دانلود نسخه تمام متن مقالات انگلیسی
امکان دانلود نسخه ترجمه شده مقالات
پذیرش سفارش ترجمه تخصصی
امکان جستجو در آرشیو جامعی از صدها موضوع و هزاران مقاله
امکان دانلود رایگان ۲ صفحه اول هر مقاله
امکان پرداخت اینترنتی با کلیه کارت های عضو شتاب
دانلود فوری مقاله پس از پرداخت آنلاین
پشتیبانی کامل خرید با بهره مندی از سیستم هوشمند رهگیری سفارشات