Efﬁcient parasitic-aware hybrid sizing methodology for analog and RF integrated circuits

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ARTICLE INFO

Keywords:
Circuit sizing
Many-objective evolutionary algorithm
Floorplan optimization
Geometric programming
Parasitic modeling

ABSTRACT

In this paper, a highly efﬁcient parasitic-aware hybrid sizing methodology is proposed. It involves geometric programming (GP) as the ﬁrst phase, both single-objective and many-objective evolutionary algorithms (EA) as the second sizing phase. The circuit performance constraints and layout-induced parasitics are considered simultaneously right from the GP sizing phase, while the optimization accuracy is signiﬁcantly improved in the EA sizing phase. The proposed methodology features an effective integration of layout information into both sizing phases. It has been used to optimize several high-performance analog and RF circuits in different CMOS technologies. The experimental results demonstrate high efﬁcacy of our proposed parasitic-aware hybrid sizing methodology.

1. Introduction

To achieve high-speed and low-power operation, the complementary metal oxide semiconductor (CMOS) technology is continuously scaled down. However, the newer technologies are associated with some drawbacks, such as strong impact of parasitics, short channel effects, interconnection issues, etc. Thinner interconnects may produce unwanted larger resistance, and closely spaced interconnects can cause an increase of coupling capacitance. Especially for the nanometer technologies, parasitic resistance and capacitance may drastically affect circuit performance [1].

Even though the portion containing analog circuitry is usually smaller than the digital one in terms of silicon area in the modern System-on-Chip solutions, the design of the analog/RF part stays as a bottleneck of the whole system design. Thus far, analog/RF circuitry has not largely beneﬁted from the mature hardware description language synthesis just as its digital counterpart. As a matter of fact, the analog/RF circuitry design is a creative and intuitive process that requires a clear understanding of circuit components and their matching requirements. Thus, it is knowledge intensive and complex in nature. It is often diﬃcult to ﬁnd a single solution that can satisfy all the analog constraints.

Most of the traditional approaches undertaken to automate the analog/RF circuit sizing are based on some sort of statistical or deterministic algorithms with the aid of ﬁtness function evaluation, which demand high computational eﬀort especially if considering the layout-induced parasitic eﬀects. The work reported in this paper aims to resolve this problem by automating the analog/RF circuit sizing in two phases. A very fast global-view GP search is conducted in the ﬁrst phase, on top of which a reﬁnement EA-based second phase can be followed. The parasitic eﬀects are taken into account throughout both circuit sizing phases.

This paper is organized as follows. Section 2 discusses some existing layout-aware circuit sizing methodologies and state-of-the-art evolutionary algorithms. A detailed description of the proposed two-phase hybrid sizing methodology is presented in Section 3. The Geometric Programming (GP), Diﬀerential Evolution (DE) algorithm, and many-objective Theta-Dominance-based Evolutionary Algorithm (θ-DEA) associated with their modiﬁcations for analog/RF sizing problems are discussed in Section 4. Section 5 mainly discusses the techniques of parasitic-awareness handling for sizing algorithms. The GP modeling for parasitic-aware sizing is discussed in Section 6 along with sizing and veriﬁcation experimental results of several typical analog/RF circuits. Finally, Section 7 draws conclusions of this work.

2. Survey of the previous works

2.1. Review of the parasitic-aware sizing

A naive parasitic-inclusive sizing method can be divided into two phases: a sizing phase for determining device sizes and biasing conditions...
in the circuitry with either a simulator or numerical fitness (or called cost) function, and a parasitic estimation phase either from actual layout or by estimation/extrapolation. That is to say, the sizing and parasitics consideration are normally done in two phases inside a nested loop. Dessouky et al. [2] proposed a trial-and-error based method by using a tool called COMDIAC, which applies the equations already defined from the detailed knowledge of a circuit. At each step, a layout tool is called multiple times to generate parasitic estimation and a circuit sizing tool responds to the estimated parasitics by changing transistor sizes. This method may have problems on loop termination in newer CMOS technologies since the parasitics may deviate a lot even for a small change in sizing. In Ref. [3], another layout-aware circuit synthesis process based on DE and a pre-formulated fitness function was proposed. However, the utilized module generator may not be able to provide accurate layout parasitics without proper analytic parasitic modeling in the advanced technologies.

Agarwal et al. [4] removed the layout process from the iteration by proposing a look-up-table (LUT) macro model for parasitic capacitance estimation. To construct the LUT model, a procedural layout generator called MSL is used along with an off-the-shelf extractor. From the reported 15 min for MSL layout generation and parasitic extraction, the time for the complete synthesis is conjectured to be significantly long although it is unknown from the paper. Moreover, linear interpolation for parasitic estimation might not be accurate enough for the advanced technologies especially if lacking a good understanding of geometry variation in the formation of fringe capacitance. Ranjan et al. [5] proposed a slightly different approach by using symbolic performance models (SPM) to take equations from small-signal models. This work tends to suffer from the pre-calculated layout information that may be only valid for a fixed layout template. In Ref. [6], the worst-case parasitics are found by determining a feasible region so that local changes in sizing are made. But this method still experiences a high CPU-time cost of simulated annealing (SA), off-the-shelf extractor, and correlation between local changes and varied parasitics.

Another method proposed in Ref. [7] is close to the general parasitic-inclusive synthesis approach, except for considering the parasitics from the previous runs rather than only taking single layout information for resizing the circuit. Their inclusion of device tuning, placement, and routing within each sizing iteration may cause difficult convergence of the output solutions. In another milestone method proposed in Ref. [8], HSPICE is used for performance evaluation within an SA process in the first sizing phase. Then as the second sizing phase, a deterministic technique is applied for fine-tuning of the design resulting from the previous phase. But for both sizing phases, only single-objective cost function is utilized. Habal and Graeb [9] proposed a method that uses nonlinear deterministic optimization with numerical simulation considering multiple device layout options, placement and routing. Parasitic estimation is achieved by an integral field solver. Since complete layout synthesis is included within each sizing iteration, the applied floorplans keep changing during the sizing optimization. The CPU time was reported to be 8 times of a traditional circuit sizing process.

Choi and Allstot [10] used particle swarm optimization and the adaptive SA for parasitic-aware RF circuit design. The process uses a commercial simulator along with a curve-fitting tool in MATLAB to provide parasitic-aware synthesis. However, the detail of parasitic modeling is unclear from the paper. Lourenço et al. [11] presented a floorplanning-aware analog IC sizing and optimization tool called AIDA, which includes a sizing engine by using a multi-objective evolutionary algorithm (MOEA) NSGA-II, and a layout generator AIDA-L [12]. Although this is a comprehensive tool suite, the floorplan templates as the input to the floorplanner for the best floorplan selection have to be provided by the circuit designers as a prerequisite.

2.2. Review of evolutionary algorithms

MOEAs are well-known for solving complex multi-objective problems (MOPs), which mean to include two or three objectives conflicting from each other. Pareto Front or Pareto Set, is a set of nondominated solutions, being chosen as optimal, where no objective can be improved without sacrificing another objective. Among the first in the field of analog EDA, Aggarwal and O’Reily [13] brought forth the concept of spatial locality and dimensional locality, with which an analog/RF sizing problem is usually equipped. They built up an adapted sizing engine based on NSGA-II and proposed a correlation sensitive mutation operator (COSMO). Moreover, they exploited the locality concept to enhance variable exploration capability with the aid of the circuit knowledge extracted from the first-order circuit performance equations or circuit sensitivity study. Nevertheless, no layout-related information was considered in that work.

Optimization problems with more than three objectives are commonly called many-objective problems (many-OPs), which most of the analog/RF sizing problems actually fall into. NSGA-II, as a typical implementation of MOEAs, is weak in handling many-OPs since a large number of solutions would be trapped in the first nondominated front, which leads to rich diversity but less exploitation capability. To address many-OPs, advanced many-objective EA (many-OEA) strategies have recently emerged. NSGA-III [14] stresses diversity more than convergence due to its less capability of attracting solutions towards Pareto Front (PF) in high-dimensional solution space, whereas MOEA/D [15] is able to approach PF quite well with its aggregation-function-based selection operator. However, without a smart control on the aggregation function, it might lose some valuable search regions. Therefore, by combining the merits of prevalent NSGA-III and MOEA/D, most recently Yuan et al. proposed θ-DEA [16], which is able to outperform its peers in handling many-MOPs. θ-DEA can not only preserve the diversity by maintaining the structural strength of NSGA-III, but also promote the convergence by employing the fitness evaluation scheme borrowed from MOEA/D.

2.3. Highlighted contributions

By extending our preliminary work [17], we have proposed a complete parasitic-aware GP-EA hybrid sizing method in this paper. We not only include floorplan optimization, GP modeling, and theoretical investigation on floorplan and interconnect parasitic modeling in a GP compatible way, but also explore performance enhancement by integrating single-objective evolutionary algorithm (SOEA) and many-OEA together for the sizing problems. Compared to the existing schemes aforementioned, our proposed parasitic-aware GP-EA hybrid sizing method in this paper has the following notable advantages:

- It is an effective combination between GP and EA sizing optimization. The GP-phase sizing process is fast yet can output a global optimum, if feasible [18]. This gives the simulation-based EA-phase sizing process an elitism starting point with implied circuit knowledge to help exploration convergence.
- By using device and interconnect parasitic models as well as floorplan symbolic constraints backed by our proven Theorem, the proposed method provides more holistic parasitic estimation much faster than any actual layout generation or procedural layout generators typically used in the conventional nested sizing-loop.
- Rather than by providing a pre-defined fixed floorplan template, the integral floorplan selection is conducted by an SA-driven engine with B*-tree representation [19] according to the constraints and objectives of a specific circuit.
- To the best of our knowledge, this is the first work that applies many-objective EA in the analog sizing domain, where the single- and many-objective EAs can switch as an optimization refiner. We also propose a scheme on experimental design and analysis of single- and many-objective EAs for optimizing engineering problems.
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