Effect of interface traps for ultra-thin high-k gate dielectric based MIS devices on the capacitance-voltage characteristics

Slah Hlali a,*, Neila Hizema, Liviu Militarub, Adel Kalboussi a, Abdelkader Souifi b

a Laboratoire de Microélectronique et Instrumentation (LR13ES12), Faculté des Sciences de Monastir, Université de Monastir, Avenue de l’environnement, 5019 Monastir, Tunisia
b Institut des Nanotechnologies de Lyon – site INSA de Lyon, UMR CNRS 5270, Bd. Blaise Pascal, 7 avenue Jean Capelle, 69621 Villeurbanne Cedex, France

A R T I C L E   I N F O

Article history:
Received 25 February 2017
Received in revised form 24 June 2017
Accepted 24 June 2017
Available online xxxx

Keywords:
Al2O3/Si interface
High-k
Metal/insulator/semiconductor (MIS)
Numerical simulation
Interface state density
C-V characteristics

A B S T R A C T

The impact of states at the Al2O3/Si interface on the capacitance-voltage C-V characteristics of a metal/insulator/semiconductor heterostructure (MIS) capacitor was studied by a numerical simulation, by solving Schrödinger-Poisson equations and taking the electron emission rate from the interface state into account. Efficient computation and accurate physics based capacitance model of MOS devices with advanced ultra-thin equivalent oxide thickness (EOT) (down to 2.5 nm clearly considered here) were introduced for the near future integrated circuit technology nodes. Due to the importance of the interface state density for a low dimension and very low oxide thickness, a high frequency C-V model has been developed to interpret the effect of interface state density traps which communicate with the Al2O3/Si and their influence on the C-V characteristics. We found that these states are manifested by jumping capacity in the inversion zone, for a density of interface, higher than \(1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}\) during a p-doping of \(1 \times 10^{18} \text{ cm}^{-3}\). This behavior has been investigated with various doping, temperature, frequency and energy levels on the C-V curves, and compared with the MIS structure that contains a standard SiO2 insulator.

© 2017 Elsevier Ltd. All rights reserved.

1. Introduction

Metal-oxide-semiconductor (MOS) structures play a crucial role in many devices, especially in microelectronics and optoelectronics. The performance and reliability of MOS devices are strongly dependent on the formation of insulator layer (native or deposited), interface states \(N_s\) localized at the semiconductor-insulator interface and the series resistance \(R_s\). The electrical and dielectric properties of these devices strongly depend on the applied voltage, frequency and temperature.

The continued reduction of device size has now necessitated the diminution of the thickness of the gate oxide layer to a few nanometers in order to maintain the same degree of gate control over the channel from a high leakage current [1]. In order to surmount this limitation, high-k (high dielectric constant) materials are being introduced to achieve a greater physical thickness and thus reduce the direct tunneling current while retaining a low oxide thickness [2,3]. Thus, replacing SiO2 with high-k materials is the prime technological challenge. In recent years there has been a growing interest in metal oxides as dielectric materials for gate oxides of MOSFETs and stable capacitors in ultra large scale integrated electronic circuits (ULSI). Extensive research is now in progress to find another insulator with a higher dielectric constant, large band gap, significant conduction band offset and high breakdown strength for use in sub-100 nm silicon technology [4,5]. New dielectric conductor combinations should be tuned for the right metal work function as well as the optimum thermo-chemical stability of the layer stack. Hence, much effort has been made to explore new combinations of dielectric and conductive layers so that miniaturization of MOS-based devices can be continued following Moore’s law. The combination TiN/Al2O3 has been identified as a promising and especially reliable candidate thanks to its chemical compatibility and thermal stability, good adhesion properties on various substrates, and low interface trap densities in TiN/Al2O3/p-Si devices [6]. Furthermore, both materials can relatively easily synthesized by atomic layer deposition (ALD) under compatible processing conditions. Al2O3 is known for its modest dielectric permittivity of ~9 and the high breakdown of electric field due to its large band gap (9 eV) [7,8]. Moreover, it has a large band offset with Si, which is crucial in maintaining low leakage currents through devices [9]. The metal TiN is a well-established midgap, with a low electrical resistance. Therefore, it is commonly used as an electrode material that blocks the out diffusion of Si more efficiently than Al.

Previously, the introduction of nanoelectronics puts a barrier in determining the nature of the MOSFETs with ultra-thin oxides as a result; nowadays it is a matter of significance to consider the interface states during MOS operation. Traps at the silicon-oxide interface play a significant role in determining the threshold voltage and inversion layer
mobility. Proper MOS device modeling requires the knowledge of the density of interface states throughout the band gap.

It is true that studies of interface states for MOS structure has required a great attraction for several years. However, scientific research in this branch of electronics continues to be attractive and fascinating among researchers today [11–14].

For example, Pengkun et al. [13] has studied the impact and origin of interface states at the monolayer MoS2 and HfO2 high-k gate dielectric interface. They found that the presence of sulfur vacancies is responsible for the generation of interface states that causes the frequency dispersion in the accumulation regime of the MoS2 MOSCAP, which exhibits a dependence on the applied gate voltage.

However, carrier transport study with an integrated high-k gate dielectric (Al₂O₃) have not been reported so far. In particular, the electrical characteristics such as capacitance-voltage (C-V) temperature dispersion and its dependence on interface states density (Dᵢ) which influence the carrier transport properties deserve a further investigation.

In this paper, the interface charge densities have been measured for MIS devices using high-k material. We have worked and analyzed on selected high-k material: Al₂O₃ the values of Dᵢ for this material and compared with the standard SiO₂ based MOS devices for constant insulator thickness.

We present a theoretical study through a bi-dimensional simulator ATLAS [15], to investigate capacitance-voltage characteristics with and without the interface state density of metal insulator (high-k: Al₂O₃) semiconductor (p-Si) devices.

We report on the effect of bias voltage, silicon substrate doping concentration and that of frequency and temperature on the electrical and dielectric properties of TiN/Al₂O₃/p-Si structure in which the Al₂O₃ dielectric layer is deposited by ALD. Our approach is based on the numerical simulation self-consistently solving the Schrödinger-Poisson equations using a finite-difference method with non-uniform mesh sizes.

2. Device characteristics

The MIS capacitor used during the simulations performed for this study is composed of a Titanium nitride gate, an Al₂O₃ insulator layer with Tₓox = 5 nm and a P-type silicon substrate with a doping concentration Nₐ = 1 × 10¹⁸ cm⁻³. The surface of our MIS structure is assumed to be 100 × 100 μm² during all bi-dimensional simulations, as presented in Fig. 2.

A DC voltage (V_c) was applied to the capacitor gate, varying from −3 V to 2 V and the AC study of high frequency C-V curve was performed, maintaining frequency at 1 kHz for all simulations.

3. Theoretical analysis

The gradual evolution of microelectronics in recent years was accompanied by a reduction in the thickness of the oxide (gate oxide in the case of the transistors), which resulted in physical or technological problems. Other oxides have been proposed and more particularly oxides with a high dielectric constant, the “high-k”. Indeed, thanks to these larger dielectric constants, one can keep a fixed oxide thickness while increasing the gate-channel coupling capacitance of the transistor [16]. To replace SiO₂, the high-k oxides must meet certain criteria in terms of the value of permittivity, band structure, discontinuity bands for the transport of loads, thermodynamic stability, quality of the interface with the Si, morphology, compatibility with the gate electrode and with the technological process, reliability, etc.

The following table (see Table 1) provides a comparison with different characteristics as dielectric constant k, band gap, conduction band (CB) offset to Si, and tunneling effective mass (m'*). The values of permittivity, band structure, discontinuity bands for these larger dielectric constants, one can keep a fixed oxide thickness while increasing the gate-channel coupling capacitance of the transistor [16].

The interface states can be estimated by measuring their densities Nᵢ using high-k oxides such as Al₂O₃ and HfO₂ high-k gate dielectric. We have worked and analyzed on these high-k oxides such as Al₂O₃ or HfO₂ high-k gate dielectric for their impact and origin of interface states at the monolayer MoS2 and HfO2 high-k gate dielectric interface.

Table 1 Material properties of SiO₂ (standard) and Al₂O₃ (high-k).

<table>
<thead>
<tr>
<th>Oxide</th>
<th>Constant dielectric K</th>
<th>Band gap [eV]</th>
<th>CB offset [eV]</th>
<th>Stability thermal compared to silicon</th>
<th>m'*/m₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂ (standard)</td>
<td>3.9</td>
<td>9</td>
<td>3.15</td>
<td>&gt;1050 °C [18]</td>
<td>0.5</td>
</tr>
<tr>
<td>Al₂O₃ (high-k)</td>
<td>9</td>
<td>8.8</td>
<td>2.8</td>
<td>&gt;1000 °C [18]</td>
<td>0.35</td>
</tr>
</tbody>
</table>

Please cite this article as: S. Hlali, et al., Effect of interface traps for ultra-thin high-k gate dielectric based MIS devices on the capacitance-voltage characteristics, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.06.056
دریافت فوری متن کامل مقاله

امکان دانلود نسخه تمام متن مقالات انگلیسی
امکان دانلود نسخه ترجمه شده مقالات
پذیرش سفارش ترجمه تخصصی
امکان جستجو در آرشیو جامعی از صدها موضوع و هزاران مقاله
امکان دانلود رایگان ۲ صفحه اول هر مقاله
امکان پرداخت اینترنتی با کلیه کارت های عضو شتاب
دانلود فوری مقاله پس از پرداخت آنلاین
پشتیبانی کامل خرید با بهره مندی از سیستم هوشمند رهگیری سفارشات