Study of the impact of electromigration on integrated circuit performance and reliability at design level

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Abstract

Electromigration damage in interconnects is a well-known bottleneck of integrated circuits, as it is responsible for the performance degradation. High values of temperature and current density accelerate the damage, causing an increase in the lines resistance and circuit lifetime reduction. In this work, a method is proposed to evaluate the electromigration effects in an operational amplifier circuit performance due the void growth induced by electromigration. The performance parameters are simulated by AC, DC and transient analysis for a specific temperature and time interval and the results are compared with a circuit free of electromigration. The method is used to investigate the circuit response regarding the unit gain frequency, voltage gain, cutoff frequency, output swing voltage and settling time. There are three lines that can be traditionally classified as critical due to the large current density they carry. Nevertheless, a fourth line, which has a current density below the maximum limit set by the technology being typically considered as non-critical from the layout design point of view, leads to significant reduction of the voltage gain and voltage swing, of about 59% and 14% in 5 years.

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1. Introduction

With technology scaling, the evaluation of the interconnect reliability regarding electromigration (EM) becomes more challenging for integrated circuit (IC) designers. To guarantee the interconnect reliability and, as a consequence, the IC reliability, traditional methods based on the Blech Effect [1] and on the maximum allowed current density are implemented during interconnect design [2]. These methods, however, do not take into account the impact of EM on the circuit performance. Interconnect reliability is normally based on results from EM tests with single lines, under extreme conditions of temperature and current density. These results are used to define the maximum current density a line should carry for a given technology and this threshold is considered in the process of chip design and interconnect sizing.

In this work, we present a method to simulate the effect of interconnect degradation due to EM in integrated circuits at design level. The temperature influence and the EM-induced void growth are correlated with the performance change of an operational amplifier. The method is applied first to analyze the transistors characteristics, transconductance and threshold voltage. Then, the amplifier performance is evaluated considering its unit gain frequency, voltage gain, cutoff frequency, output voltage swing and settling time. Based on such an investigation the critical lines are determined for each of the above parameters and compared with the critical lines obtained from a traditional EM tool, that is based on the maximum current density check only.

2. Interconnect design and EM analysis

The Blech product criterion [1], expressed by Eq. (1), indicates if a single line is prone to failure, based on the maximum stress the conductor line can withstand \((\sigma_m)\), initial stress \((\sigma_0)\), atomic volume \((\Omega)\), valence number \((Z)\), electron charge \((e)\), and line resistivity \((\rho)\).

\[
(jL_e) = \frac{\Omega(\sigma_m - \sigma_0)}{2Zep}\ .
\]  

(1)

The maximum current density is a criterion used to size the width of interconnects in an IC. Both criteria are used to infer the line reliability under EM from a design point of view. Fig. 1 shows the boundaries for interconnect design, given by the typical Blech product values for Cu (0.37 A/μm) [2] and Al (0.1 A/μm) [3], and the critical current density for Metal 1 lines of a 45 nm technology (2 mA/μm or 13.3 mA/μm², as the Cu line height is 150 nm) [4].

The line resistance under EM varies by [5]

\[
\frac{\Delta R(t)}{R_0} = \left( \frac{\rho_b}{\rho} \frac{A}{A_b} \right) \frac{L}{L_b},
\]

(2)
where $R_0$ is the initial line resistance, $\rho_b$ is the barrier layer resistivity, $A$ is the line cross section, $A_b$ is the barrier cross sectional area, and $L$ is the line length. The void length, $l_v$, is calculated by

$$l_v(t) = \frac{D e Z}{k T} j(t)$$

(3)

Table 1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Ref</th>
</tr>
</thead>
<tbody>
<tr>
<td>TaN barrier area</td>
<td>$A_0$</td>
<td>$3.0E-15 + wE-8$</td>
<td>m$^2$</td>
<td>[4]</td>
</tr>
<tr>
<td>Cu line area</td>
<td>$A$</td>
<td>$15wE-8$</td>
<td>m$^2$</td>
<td>[4]</td>
</tr>
<tr>
<td>Cu diffusivity$^b$</td>
<td>$D_0$</td>
<td>$3.1E-5$</td>
<td>m$^2$/s</td>
<td>[9]</td>
</tr>
<tr>
<td>Cu diffusivity$^b$</td>
<td>$D$</td>
<td>$D_0 \exp (\frac{-\Delta}{k T})$</td>
<td>m$^2$/s</td>
<td>-</td>
</tr>
<tr>
<td>Cu resistivity$^b$</td>
<td>$\rho_c$</td>
<td>$24E-9$</td>
<td>Ω·m</td>
<td>[7]</td>
</tr>
<tr>
<td>Cu resistivity$^b$</td>
<td>$\rho$</td>
<td>$\rho_c (1 + \alpha \Delta T)$</td>
<td>Ω·m</td>
<td>-</td>
</tr>
<tr>
<td>TaN resistivity</td>
<td>$\rho_{a0}$</td>
<td>$135E-9$</td>
<td>Ω·m</td>
<td>[9]</td>
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<tr>
<td>TaN resistivity</td>
<td>$\rho_a$</td>
<td>$\rho_a (1 + \alpha \Delta T)$</td>
<td>Ω·m</td>
<td>-</td>
</tr>
<tr>
<td>Cu temp. coeff.</td>
<td>$\alpha$</td>
<td>$4.3E-3$</td>
<td>1/K</td>
<td>[9]</td>
</tr>
<tr>
<td>TaN temp. coeff.</td>
<td>$\alpha_b$</td>
<td>$3.5E-3$</td>
<td>1/K</td>
<td>[9]</td>
</tr>
</tbody>
</table>

$^a$ $w$ = line's width.

$^b$ $T = 293$ K.

The IC performance changes are evaluated due EM effects for a time interval and specific temperature. AC, DC and transient analysis are performed to study the variations of the circuit parameters. The results are compared with the obtained with the VEAD, an electromigration Cadence tool that classifies the lines as critical based in the current density threshold from technology [8].

4. Results

We apply the proposed method to investigate the EM effect on the performance of an operational amplifier (Opamp). This amplifier contains 20 transistors and 15 interconnects. It is designed to have 40 dB gain for 1 MHz, unit gain frequency (UGF) of 730 MHz, output voltage swing of 2.2 V and maximum settling time of 10 ns, at 125 °C. The amplifier is fed by a 1.3 V differential voltage ($|avdd| = |avss| = 0.65$ V). It is designed in a 45 nm technology, which is composed by three metal layers (M1, M2, and M3) of Cu using a TaN barrier layer. M1 has a minimum width of 60 nm, while M2 and M3 have 80 nm [4]. Fig. 3 shows the operational amplifier schematics and Fig. 4 presents the designed layout of the IC.

The "avdd", "avss" and "outp" lines are subjected to the highest "current densities" (here, design nomenclature – current per width – will be used throughout the text), above 2 mA/μm, as simulated with EAD Cadence tool. The measured current for avdd line is 3.1 mA, which given the line dimensions, represents a maximum current density of $j$ is the current density, $D$ is the atomic diffusivity, and $k$ is Boltzmann's constant.

In this study, the Cu diffusivity is calculated for an activation energy ($E_a$) of 1.0 eV. In Table 1, the Cu line and TaN barrier have cross sectional areas as function of the line width ($w$). The minimum width is 60 nm for the 45 nm technology [5].

Normally, a resistance increase of 10% is used as failure criterion for an interconnect line [6]. However, the performance of the circuit is not necessarily affected by such a criterion and a more complex analysis is required to relate the interconnect and the circuit reliability. Therefore, an investigation of the EM impact on the circuit operation as a line resistance changes is crucial for a circuit reliability evaluation. Furthermore, this analysis allows the designer to find the critical lines of a given design, where complex structures with multbranches and parallelisms are present.

3. Evaluation of the EM effect in IC performance

Fig. 2 illustrates the methodology flow to evaluate the EM effect on IC performance. In order to perform the EM analysis, the circuit schematic and the layout of the design are required. First, from the schematic, the current values (Idc) of each line are simulated. In turn, the widths of the lines are extracted from the layout. These values are then used to determine the line current density, so that the void length is calculated using Eq. (3) and the resistance variation ($\Delta R$) of each line can be determined with Eq. (2). Once the $\Delta R$ is known, it can be added to the initial interconnect resistance. Finally, the circuit is again simulated and its performance, defined by a given parameter or set of parameters, is compared to the performance of the circuit without the EM effect. For this analysis, Cadence Design tools in conjunction with external tools are used.

The IC performance changes are evaluated due EM effects for a time interval and specific temperature. AC, DC and transient analysis are performed to study the variations of the circuit parameters. The results are compared with the obtained with the VEAD, an electromigration Cadence tool that classifies the lines as critical based in the current density threshold from technology [8].
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