

# Data rate enhancement of optical camera communications by compensating inter-frame gaps



Duy Thong Nguyen, Youngil Park\*

School of Electrical Engineering, Kookmin University, Seoul 136-702, South Korea

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## ABSTRACT

Optical camera communications (OCC) is a convenient way of transmitting data between LED lamps and image sensors that are included in most smart devices. Although many schemes have been suggested to increase the data rate of the OCC system, it is still much lower than that of the photodiode-based LiFi system. One major reason of this low data rate is attributed to the inter-frame gap (IFG) of image sensor system, that is, the time gap between consecutive image frames. In this paper, we propose a way to compensate for this IFG efficiently by an interleaved Hamming coding scheme. The proposed scheme is implemented and the performance is measured.

## 1. Introduction

Recently, broadband communications technology and its services are developed rapidly. The number of devices used for broadband services is increasing also, that leads to the overload of bandwidth and speed limitation in RF-based communication technology. From a decade ago, visible light communications (VLC) has appeared and regarded as a way to solve this bandwidth shortage problem. This technology uses LED lamps in illumination and communication at the same time. As with the deployment of LED lamps in many places, this VLC technology will play an important role in the provision of Internet-of-Things (IoT) infrastructure. Optical camera communications (OCC) is a part of the VLC technology, which uses image sensors as a receiver. As most smart devices such as smart phone, tablet PC, black box of vehicles have integrated high quality camera, users can take photo or video easily. In addition, light emitting diodes (LED) are used as transmitter with low power consumption, long lifetime, low cost and can be easily integrated with the light system. Therefore, OCC is expected to replace the traditional RF communication technology.

Several schemes have been studied to enhance the performance of the OCC. Firstly, a high-quality camera has been used to achieve the high performance by controlling the parameters such as resolution, expose time, inter frame gap, frame rate, etc. Secondly, LED arrays have been tried to carry multiple data bits at the same time [1]. Thirdly, a rolling shutter mechanics of a CMOS image sensor have been used to receive multiple data bits in a single image frame [2–6]. Among these three approaches, the rolling shutter based OCC scheme has been tried by many research groups since it is easily implementable using low-

price image sensor devices. In this OCC scheme, however, there exists a time gap, called inter-frame gap (IFG), between consecutive frames; this IFG limits the data rate seriously since image sensors can't receive data in this time period. To avoid the bit loss in the IFG, each packet is transmitted twice so that at least one of them is received completely. Although this process can compensate for the bit loss, the data rate of this OCC scheme is reduced to half. Therefore, in this paper, we propose a new way to avoid this duplicate packet transmission by employing Hamming coding and bit interleaving. Although Hamming coding can correct a single error bit, it can't correct the bit loss in the IFG since the time period of the IFG exceeds one-bit period. Therefore, bit interleaving is used to scatter the error bits occurred in the IFG.

In the rest of this paper, the detailed coding schemes for the IFG compensation as well as the data packet structure are provided in Section 2, while the performance is analyzed and compared with that of the existing scheme in Section 3. The experiment results are shown in Section 4. And finally, the conclusions and discussions of the study are presented in Section 5.

## 2. Rolling shutter based OCC scheme and its limitation

A CMOS image sensor becomes more common in most digital cameras since this technology has leapfrogged Charge Coupled Devices (CCD). Although there are similarities between these two devices, a major difference is the way that each device collects the information from pixels. For the CCD, all rows are exposed at the same time and as the exposure is complete, information from each pixel is readout in sequence. By the way, the CMOS sensor avoids bottleneck by exposing

\* Correspondence to: Kookmin University, School of Electrical Engineering, 77 Jeongneung-Ro, Seongbuk-Gu, Seoul 02707, South Korea.  
E-mail address: [ypark@kookmin.ac.kr](mailto:ypark@kookmin.ac.kr) (Y. Park).

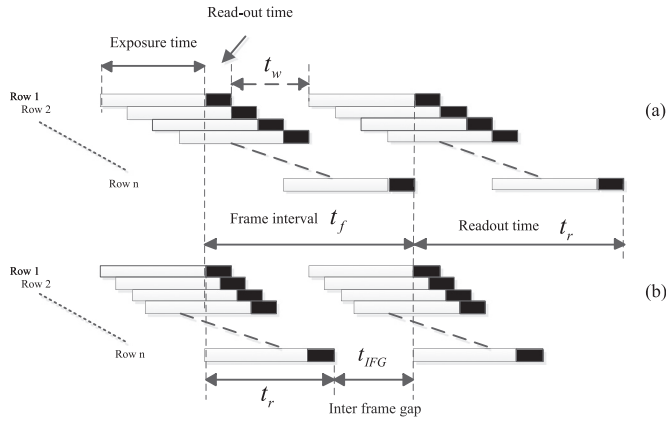


Fig. 1. Processing of consecutive frames in a CMOS image sensor (a) Ideal system (b) Practical system.

and readout each row in sequence; it is called a rolling shutter mechanism. In this process, the time difference between two adjacent rows equals the readout time, allowing no IFG between two frames although overlapped exposures are seen among rows [7] as illustrated in Fig. 1(a). In this case, the frame rate is determined by the multiplication of readout time and the number of rows in an image sensor. Each row of the next frame waits for  $t_w$  to make sure that readout process in the current frame is finished before the readout in the following frame begins. The overlapped readout process in different rows is possible since each row has its own A/D converter in the CMOS image sensor.

In commercial CMOS image sensor, however, there is a “free” time between two adjacent frames, which is necessary to combine all rows in a frame to form a single image [3], or to prepare for the next frame, as well as other purposes [2]. According to [8], readout time corresponds to 60–90% of time interval between frames. This time gap between the frame interval and the total readout time is called a inter frame gap  $t_{IFG}$ , as shown in Fig. 1(b). The frame interval  $t_f$  and the frame rate  $F_r$  are calculated as:

$$t_f = t_r + t_{IFG} \tag{1}$$

$$F_r = \frac{1}{t_f} = \frac{1}{t_r + t_{IFG}} \tag{2}$$

The frame interval,  $t_f$ , is measured as shown in the Fig. 2. The average value is about 33 ms, making the frame rate approach 30 fps. However, periodic peaks are shown, which is attributed to the image processing time in a camera. It is hard to separate  $t_r$  and  $t_{IFG}$  from this result only since they depends on image sensors and environments.

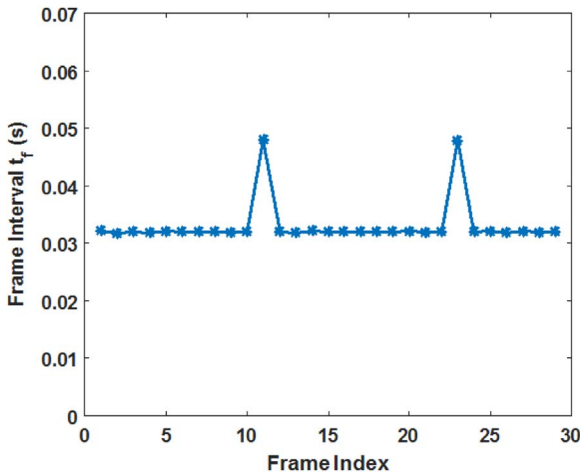


Fig. 2. Measurement of the frame interval ( $t_f$ ).

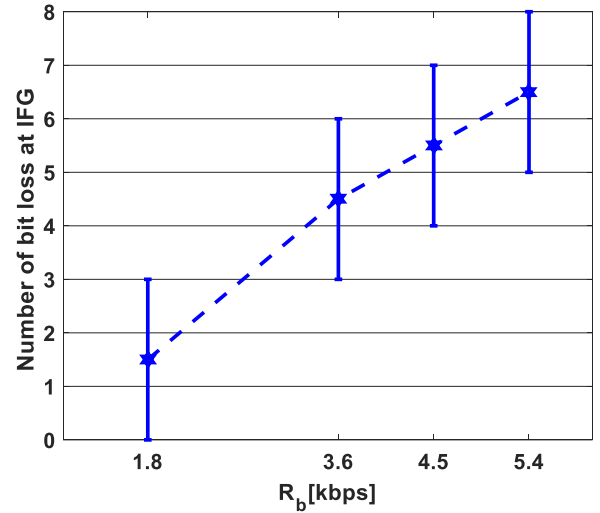


Fig. 3. Relationship between data rate and bit loss in the IFG.

To measure the IFG more precisely, we transmitted bit sequence using an LED and a CMOS image sensor in various data rate. Lost bits due to IFG can be easily counted by the comparison of Tx and Rx data, and the results are illustrated in Fig. 3. From this figure we can calculate the IFG by considering the bit period and the lost bit numbers. It is calculated that the IFG varies in the range of 0.8–1.7 ms. This result is used as an important reference when the proposed coding scheme is designed in Section 3.

Modulation frequency of LED should be high enough to avoid the flickering, but should be lower than the shutter speed of the camera to acquire enough exposure time in each row. Considering these requirements, LED modulation frequency for OCC must be in the range of 200 Hz and 8 kHz [4]. However, it is difficult to increase the data rate above a certain amount since higher data rate causes more bit loss at the same amount of IFG.

### 3. Proposed block coding for OCC

As mentioned in the previous section, one of the problems that limits the rolling shutter based OCC is the time gap between frames. Cameras cannot receive data in this period. Existing schemes solves this problem by transmitting data twice to compensate for the possible data loss [3–6], which reduces the final information rate to half. To overcome this problem, we propose a new scheme using block coding and bit interleaving as shown in Fig. 4. Data rate can be enhanced by using this scheme since duplicate data transmission is not used anymore. In order to compensate for the bit loss in the IFG, the number of lost bits are measured and the same number of random bits are inserted in this time gap. Then, Hamming code is used to correct the error bits placed among the random bits. In this scheme, (7,4) Hamming coding that can correct one-bit error is used to convert the ASCII data. Since this Hamming code can't correct multiple error bits in the same coding block, however, bit interleaving is used to scatter the error bits. Fig. 5 shows this process, where each Hamming block is placed in each row, while bits are transmitted in the sequence of each column. Therefore, bits in the same Hamming block are not transmitted continuously, and as a result, multiple errors due to the IFG do not belong to the same Hamming block. For this purpose, the number of Hamming blocks used in the bit interleaving should be larger than the estimated number of lost bits in the IFG. If six Hamming blocks are used as shown in the Fig. 5, then the lost bits should not be above six for appropriate compensation. It is seen from Fig. 3 that the data rate up to 3.6 kbps can be used with this structure. If more Hamming blocks are employed in the bit interleaving, then the data rate higher than 3.6 kbps can be implemented.

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