1. Introduction

Almost all electronic systems today have a significant digital part, which must interact with analog variables of the external world. Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) are therefore a fundamental part of any electronic system, with a key role in performance and price figures.

Designing ADCs is a matter for few specialized engineers, while using ADCs is something every electronic system designer has to deal with. A good understanding of principles and techniques of A/D conversion is mandatory to select the most suitable device - or combination of existing devices - for the specific application. In this context teaching ADC Architectures means to provide the ability to make motivated choices at the system level, rather than analyze the design details of specific circuits.

ADCs are often presented in textbooks as a collection of circuits with different performance, optimizations, and tradeoffs for speed, precision, cost. Several papers, textbooks, and manufacturers tutorials [1, chapter 9.9], [2, chapter 16.5], [3, chapter 16.14], [4, chapter 10.4], [5,6, chapter 13] discuss sample circuits, in some cases down to the transistor level. This approach leads to the knowledge of existing classic architectures and devices, but does not present a general view of the many possible choices. Discussions of the evolution of ADCs and the description of several top-performance structures with emphasis on critical aspects are in a theme issue of the IEEE Solid State Circuits Magazine and in several other journals [7-13].

This paper identifies and compares parameters and features of each ADC type, in order to define a frame for teaching and for motivated selection. This approach leads to a structured taxonomy for classic architectures, and shows how the wide variety of ADC circuits can be derived from few basic techniques. The result is an ample design space, where available commercial ADCs represent some reference points, but a skilled system designer can exploit many additional solutions to improve performance or to optimize specific parameters.

The aim is to make the system engineer understand where tradeoffs are, which are the actual degrees of freedom, where to intervene for optimization. This approach to ADC has been followed for several years in various courses at Politecnico di Torino, it is used in a book [14] and in on-line courses [15].

2. Course context and structure

In BS degrees at Politecnico di Torino Analog to Digital conversion is introduced in the third year in various Information Technology curricula: Electronics, Computer Engineering, Telecommunication. More design details are provided in the Electronic Engineering Master level degree. Before receiving these contents the students get courses on analog and digital electronics, signal theory, and use measurement instruments in the lab. The set of lessons on Analog/Digital conversion is organized in several sections:

1. general principles of A/D and D/A conversion;
2. DAC parameters, errors, taxonomy, circuits;
3. basic ADC parameters, errors, taxonomy, circuits;
4. special ADC structures (residue, pipeline, ...);
5. ADC for specific applications (ΔΣΔ, log, ...);
6. signal conditioning (amplifiers, filters, mux, S/H, ...).

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Overall time span ranges from 9 to 15 room hours, plus one to three laboratory sessions with measurements on real circuits. The learning material includes a reference textbook [14] and the course websites with slides and instruction for lab experiments (e.g., [16], Section D). This paper details the issues described in Sections 3 and 4 of the previous list.

3. A/D conversion parameters

An ADC should provide the digital output from the analog input in a negligible amount of time, with a high number of (correct) bits, use very little power, and fit in a small silicon area. An ideal converter that fulfills all these requirements does not exist: each specific ADC structure optimizes different parameters. The teaching path here described shows how each design solution leads to the optimization of a specific aspect, usually at the expense of the others.

The first introductory lesson defines two parameters as the most significant for an ADC: the conversion delay, defined as the time required to get the final digital value, and the circuit complexity, related to the number and/or area of devices in the circuit. The conversion time of an Analog to Digital Converter is heavily affected by the performance of its core element, the voltage comparator [17–19]. In the present taxonomy, to avoid depending on parameters which vary depending on technological improvements, performance and costs are evaluated with respect to the following normalized parameters:

- \( \tilde{t} \), conversion delay normalized to the delay of a single comparator (time required for a single-bit decision);
- \( c \), complexity (indicated as cost in the parameter tables) normalized to the complexity of a comparator.

In this way, the delay is defined by the number of sequential decisions in the conversion process, and the complexity by the number of comparators used in the circuit. Using these two numbers, the following analysis shows how the various techniques and circuits represent different tradeoffs for speed and cost (or complexity) in the design space.

Two other parameters that are used throughout this paper are the input signal full dynamic range \( S \) and the number of bits \( N \) produced by the conversion. Without loss of generality, we assume the conversion is linear and thus the input is divided into \( 2^N \) equal intervals, each corresponding to one LSB in the digital output.

All ADC architectures are also subject to various errors: Gain, Offset and Non-linearities are the most representative. Gain and offset can be corrected with proper calibration [20,21]. Differential and Integral nonlinearity errors (DNL, INL) depend on the ADC structure, such as those presented in Section 4, and on the behavior of the internal DAC for feedback ADCs. Structures with a single reference (e.g. differential and integrating) have intrinsically good DNL, because 1 LSB step is unique. Structures which combine multiple quantities (e.g. weight network DAC) may have worse DNL.

While previous errors are measured in DC, other kind of errors manifest themselves in the frequency domain, as unwanted contributions to the sampled signal power spectrum. They are usually identified by specifying the Signal-to-Noise and Distortion (SINAD) ratio, which is the ratio between the power of the signal and the power of the noise, including harmonics, or by the Spurious Free Dynamic Range (SFDR), which is the ratio between the power of the signal and the power of the strongest noise contribution in the spectrum, generally given in dBs. A good indication of the quality of the converter is the Effective Number of Bits (ENOB), which is computed by considering all possible error sources. Architectures that exploit parallelism to improve performance may show worse figures with respect to these errors, because component matching becomes harder.

Power consumption parameters are not considered in this taxonomy because they are more related to the actual usage speed and to the adopted technology. In general, converters dedicated to high frequency applications, and hence having a low conversion delay, show a higher power consumption than slower converters, which, on the other hand, often achieve a better resolution [22]. However, exploiting the power down feature of a fast converter in a slow acquisition system can result in lower average power consumption. Moreover, for all presented architectures, lower power can be achieved with capacitive weight networks.

4. Classic ADC architectures

The classic types of A/D converters (flash, successive approximation, differential) are here presented and positioned in the design space. This generates a first cost/speed table and allows identifying other types of converters (Section 5).

4.1. Flash ADC

The basic structure of a Flash converter is in Fig. 1. A multiput voltage divider creates thresholds that define the input intervals, then a number of voltage comparators and an encoder produce the final digital output. To identify which one of the \( 2^N \) intervals includes the input, \( P = 2^{N-1} \) comparators are required; the normalized complexity of this structure is therefore proportional to \( 2^N \). Since all comparators examine the input signal in the same time slot, the total conversion time corresponds to a single comparator delay.

4.2. Feedback ADCs

The next types of ADC are based on a feedback loop, which includes a comparator, an approximation logic, and a DAC. The input signal to be converted is compared to the output voltage of the DAC, driven by the approximation logic. In turn, the outcome of the comparison guides the approximation logic. The process is iterated a number of times to reach the desired accuracy of the result. This basic scheme applies to staircase, tracking, integrating, differential and successive approximation converters. The key difference is the approximation algorithm driving the DAC: 1 LSB steps for the staircase, tracking, integrating and differential ADCs, variable steps (starting from MSB) for the successive approximation ADC.

The Staircase converter (Fig. 2(a)) uses a counter, cleared at conversion start and incremented until the DAC output \( A' \) crosses the input \( A \). The system uses only one comparator; the complete dynamic range \( S \) is explored in \( 2^N \) steps, 1 LSB each. Complexity is at the minimum, but the conversion delay is at maximum (\( 2^N \) sequential decisions in the worst case). With a bi-directional counter the circuit can track slow changes in the input signal; it becomes a Tracking ADC.

Integrating converters replace the \(<\text{counter} + \text{DAC}>\) units with \(<\text{integrator}>\). A variation of this technique, with multiple ramps to correct analog errors such as the comparator offset, is often used in DVMs [23].
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