Power efficient synchronous counter design

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Abstract

The Performance of any VLSI circuit depends on its design architecture, which optimizes power and provides high reliability. To design any circuit with low power, power optimization of circuit at different levels is needed. Most of the system level architectures consists of sequential circuits, design of these circuits plays a pivotal role in reducing overall power of the system. Counters are basic building blocks in many VLSI applications such as timers, memories, ADCs/DACs, frequency dividers etc. It is observed that design of counters has power overhead because of requirement of high power consumption for the clock signal distribution and undesired activity of flip-flops due to presence of clocks. In this brief, we propose a power efficient design of synchronous counters that reduces the power consumption due to clock distribution for different flip-flops and offers high reliability. The proposed counter design is evaluated and analyzed in terms of power in a standard 45 nm CMOS technology in CADENCE and also evaluated in Synopsys Design Compiler and IC Compiler for ASIC (Application Specific Integrated Circuit) synthesis results. The proposed counter design has lower power requirement and power-area product than existing counter architectures and the power reduction is more significant for wide-bit counters.

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1. Introduction

Most of the computer processes are synchronized with clock cycle, so sequential circuit has major contribution in many VLSI circuits. Thus design of sequential circuits with minimum power is a crucial factor in VLSI design and for high performance applications, it plays an important role.

Power consumption is an important characteristic when it comes to portability and mobile devices. Power consumption is a serious concerning matter in recent time, because of high frequencies and size of chips [2]. The major power contribution in any circuit is due to static and dynamic power dissipation. Static power dissipation occurs in quiescent state of circuit due to sub threshold conduction, reverse biased pn junction conduction, gate tunneling current, drain source punchthrough, gate induce drain leakage etc. However, the contribution of static power is low when compared to dynamic power.

Dynamic power dissipation occurs due to transition of signal and short circuit current [2]. Short circuit power dissipation is due to momentary shorting of power supply and ground during signal transition. The contribution of short circuit power is about 5–10% of dynamic power. The power consumed due to signal transition from low-high and high-low contributes major portion of dynamic power [1,2].

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Counters are the basic building blocks in many VLSI systems. A ‘k’ bit binary counter can count $0 – (2^k – 1)$ and consist of series of k-flip flops [1]. Design of the counters with low power consumption and high reliability is utmost important especially as it is operated by clock. The major power contribution in counters is due to clock which has high load from its driving nets. Also, this clock is always present across all flip flops which are not active, contributing large power overhead on designs. It is observed that clock signals in counter applications consumes on average of 25–40% of the total power [2]. Thus, the circuit power can be greatly reduced by reducing the clock power dissipation.

Counters are mainly categorized into synchronous and asynchronous counter based on clock triggering. In synchronous counter the clock pulse to the flip-flops are given at same time from single master clock, whereas in asynchronous counters the first flip flop receive clock pulse from the master clock and the output of the first-flip flop will act as the clock pulse to the next flip-flop and so on. Asynchronous counters are usually restricted by large propagation and may become unreliable at higher clock frequencies [1,2]. A high speed and power efficient asynchronous ripple counter is presented in [11] which overcomes large propagation delay by using a novel single edge triggered D flip-flop, but [11] is restricted by maximum operating frequency. However, synchronous counters operate at high speed and more reliable because of its usage of same clock across all flip-flops which ensures all outputs are changed simultaneously. Thus synchronous counters are most frequently used counters in many designs because of its deterministic behavior and low design complexity [1].

There are several efficient counter architectures available in literature which has power optimization at different levels [3–17]. A low power counter based on priority encoding is presented in [4], which is based on compressing multiple binary inputs into outputs. A Ring counter which is based on replacing flip-flops with pulsed latch is presented in [5]. However, [4,5] requires additional hardware interms of priority encoder and pulse generator, which imposes restriction on design complexity for wide-bit counters.

A quasi-synchronous based counter design which optimizes the power dissipation is presented in [6]. Here a quasi-synchronous clock is derived from the master clock, which isolate the flip-flops in the circuit from the unwanted transitions, thereby minimizing power consumption. An extended true single phase clock based counter is presented in [7], which uses new OR scheme using single transistor to implement counting logic. A new toggle reduced counter which works on low activity quasi clock is presented in [8]. Although [6–8] presents efficient counter architectures based on deriving novel clocking schemes, however they are restricted by large layout and requirement of clock generation circuit.

A low power binary counter using bistable storage elements which is based on irreversible semi-static CMOS is presented in [9]. However [9] is restricted with additional hardware overhead and requirement of generating two phase non-overlapping clocks. A high speed binary counter based on 1D Cellular Automation is presented in [10], which works by generating a new number sequence that emulates the binary number system. Although [10] presents a very simple design based on generation logic, but it is restricted for wide-bit counters, due to information redundancy.

Several counter architectures based on adiabatic logic are presented in [12–15]. A low power counter based on adiabatic logic and complementary pass transistor logic is presented in [12,14]. An improved novel clocking based adiabatic logic is presented in [13]. A new modified adiabatic logic based on quasi static energy recovery logic is presented in [15]. Although counters [12–15] based on adiabatic logic is an effective technique which reduces the power dissipation, it is restricted by the requirement of generating complementary sinusoidal clocks that requires additional clock generating circuit at the cost of increased design complexity.

It is observed that the dominant power consumption (nearly 25%–45%) in counter applications is due to the activity of clocks. Clock gating is one of the most effective technique to reduce power dissipation by eliminating unnecessary clock activity at different levels. A low power design of counter using clock gating is presented in [16]. A power efficient design of Johnson counter using clock gating is presented in [17]. However [16,17] requires additional hardware for implementing clock gating network and inherent interconnect complexity and overhead on clock buffer network increases linearly with width of counters.

In this brief, we present a power efficient design of synchronous counters with efficient clock gating technique with minimum hardware overhead. Here a new combinational logic with minimum hardware across each input of flip-flop is designed, which eliminates clock activity when flip-flop is not active, thereby reducing high clock load and therefore power consumption. The proposed clock gating network replaces the higher hardware overhead of existing techniques with simple combinational circuit. The proposed clock gating network constitutes structured clock buffer network in an hierarchal approach for wide-bit counters.

The remaining brief is organized as follows. In Section 2 the conventional binary counter design is discussed. Section 3 presents the proposed binary counter design technique. Section 4 extends the proposed binary counter to Up-Down counter. Section 5 presents the performance comparison and analysis. Finally, Section 6 concludes.

2. Conventional binary counter design

There are many different ways to design counters, among them JK flip-flops in master-slave mode (J and K connected to 1) is used widely since JK flip-flops in master-slave mode (Toggle flip-flop) offer a way to toggle only once for clock pulse, which is the fundamental function in order to build a counter. The schematic diagram of Toggle flip-flop (T flip-flop) and 4 bit conventional synchronous binary counter is shown in Figs. 1 and 2 respectively.

For k-bit counter design, we need ‘k’ number of flip-flops. From Fig. 2, it can be observed that ‘T’ inputs of all the flip-flops are set to 1, so in every positive edge the output will be inverted. As by the nature of synchronous design all the
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