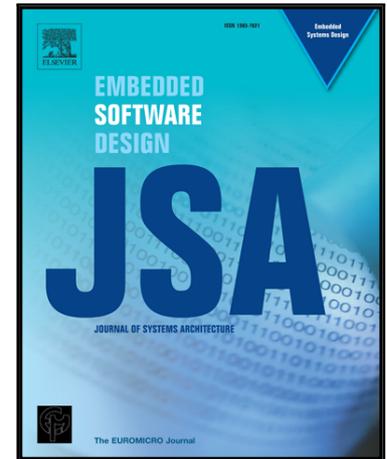


## Accepted Manuscript

Efficient Task Spawning for Shared Memory and Message Passing in Many-core Architectures

Aurang Zaib, Thomas Wild, Andreas Herkersdorf, Jan Heisswolf, Jürgen Becker, Andreas Weichslgartner, Jürgen Teich

PII: S1383-7621(17)30136-4  
DOI: [10.1016/j.sysarc.2017.03.004](https://doi.org/10.1016/j.sysarc.2017.03.004)  
Reference: SYSARC 1426



To appear in: *Journal of Systems Architecture*

Received date: 23 February 2016

Accepted date: 5 March 2017

Please cite this article as: Aurang Zaib, Thomas Wild, Andreas Herkersdorf, Jan Heisswolf, Jürgen Becker, Andreas Weichslgartner, Jürgen Teich, Efficient Task Spawning for Shared Memory and Message Passing in Many-core Architectures, *Journal of Systems Architecture* (2017), doi: [10.1016/j.sysarc.2017.03.004](https://doi.org/10.1016/j.sysarc.2017.03.004)

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting proof before it is published in its final form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

## Efficient Task Spawning for Shared Memory and Message Passing in Many-core Architectures

Aurang Zaib\*, Thomas Wild and Andreas Herkersdorf

*Technische Universität München (TUM), Germany*

Jan Heisswolf and Jürgen Becker

*Karlsruhe Institute of Technology (KIT), Germany*

Andreas Weichslgartner and Jürgen Teich

*Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany*

---

### Abstract

Modern many-core systems consist of large number of processing cores and introduce more and more parallelism. The Partitioned Global Address Space (PGAS) programming model is a popular approach for exploiting this parallelism of architectures while offering flexibility of both shared memory and message passing paradigms. On the architecture design front, Network on Chips (NoCs) have become an integral part of the communication infrastructure due to their good scalability. In order to exploit task level parallelism on modern many-core architectures, the applications spawn more and more tasks to the available computing resources. The applications require less communication and synchronization delays for better performance. However, the distributed nature of NoCs poses a challenge to keep data communication and synchronization latency within the desired bound and hence results in higher task spawning overhead.

We proposed an approach based on hardware-assisted task spawning on many-core systems Zaib et al. (2015). In the current article, we present an extended version of our work for hardware-managed task spawning, keeping in view the communication requirements of both shared memory and message passing programming models. The proposed hardware support, integrated into the network interface architecture, reduces the synchronization

---

\*Corresponding author

*Email address:* [aurang.zaib@tum.de](mailto:aurang.zaib@tum.de), [aurang.zaib@gmx.de](mailto:aurang.zaib@gmx.de) (Aurang Zaib )

متن کامل مقاله

دریافت فوری ←

**ISI**Articles

مرجع مقالات تخصصی ایران

- ✓ امکان دانلود نسخه تمام متن مقالات انگلیسی
- ✓ امکان دانلود نسخه ترجمه شده مقالات
- ✓ پذیرش سفارش ترجمه تخصصی
- ✓ امکان جستجو در آرشیو جامعی از صدها موضوع و هزاران مقاله
- ✓ امکان دانلود رایگان ۲ صفحه اول هر مقاله
- ✓ امکان پرداخت اینترنتی با کلیه کارت های عضو شتاب
- ✓ دانلود فوری مقاله پس از پرداخت آنلاین
- ✓ پشتیبانی کامل خرید با بهره مندی از سیستم هوشمند رهگیری سفارشات