GaAsSb/InGaAs tunnel field effect transistor with a pocket layer

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This work proposes a new GaAsSb/In0.53Ga0.47As heterojunction tunnel field effect transistor (HTFET) with a 6-nm In0.7Ga0.3As layer (pocket) between the source and channel. Compared with InGaAs homojunction TFETs, the proposed HTFET has a steeper subthreshold swing at a higher drain current, owing to its lower source-to-channel tunnel barrier height. It has a maximum on-state current of 11.98 μA/μm at room temperature, which is more than ten times the on-state current obtained from an InGaAs homojunction TFET.

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1. Introduction

Tunnel field-effect transistors (TFETs) based on band-to-band tunneling of carriers are promising devices because they can realize subthreshold swing (SS) of <60 mV/dec and can operate at a low supply voltage without an increase in their off-state currents [1-5]. In addition, the positive bias temperature instability (PBTI) reliability of these TFETs has been studied and compared with the PBTI reliability of a comparable InGaAs MOSFET device [6]. Reliability assessment shows that the SS and transconductance (g_m) of a TFET are more immune to PBTI stress than an equivalent MOSFET device. A review paper explored the effects of reliability issues on TFET devices and circuit performance levels [7]. Compared with MOSFETs, however, silicon-based TFETs usually have low on-state currents because of the large source-side tunneling barriers of silicon-based materials. To overcome this phenomenon, bandgap-engineered heterojunctions have been proposed [8-11]. Tunneling barriers can be tuned by implementing arsenide-antimonide heterojunctions or by inserting a smaller tunneling barrier; therefore, increased on-state current can be achieved from the increased efficiency of the band-to-band tunneling process. As demonstrated in [9], a 6-nm-thick In0.7Ga0.3As pocket can be added next to the source in an InGaAs homojunction TFET to provide a smaller tunneling barrier.

In this paper, we propose a GaAsSb/InGaAs heterojunction TFET (HTFET) with a 6-nm-thick In0.7Ga0.3As pocket inserted between a GaAsSb/In0.53Ga0.47As source and an In0.53Ga0.47As channel to lower the tunnel barrier height. At room temperature, the proposed GaAsSb/InGaAs HTFET with a pocket exhibits a higher on-state current than does an InGaAs homojunction TFET.

2. Device structure and fabrication

The device structures of In0.53Ga0.47As homojunction TFET and a GaAsSb/In0.53Ga0.47As HTFET with a pocket are illustrated in Fig. 1(a) and Fig. 2(a), respectively. As shown in [10], a lattice-matched GaAsSb/In0.53Ga0.47As HTFET at the source side can reduce the tunneling barrier from 0.74 eV in an InGaAs homojunction TFET to 0.5 eV by using a staggered type-II junction. The proposed HTFET is similar to a GaAsSb/InGaAs HTFET, with the exception that a 6-nm-thick In0.7Ga0.3As “pocket” was grown next to the source to provide a remarkably small tunneling barrier. All epitaxial layers were grown through molecular beam epitaxy on semi-insulating InP substrates and supplied by IntelliEPI Inc. The homojunction TFET consisted of a 300-nm p+ In0.53Ga0.47As source (>8×10^{18} cm^{-3}), a 150-nm-thick intrinsic In0.53Ga0.47As channel, and a 200-nm-thick n+ In0.53Ga0.47As drain (>1×10^{18} cm^{-3}). The GaAsSb/InGaAs HTFET with a pocket comprised a heavily p-type doped GaAsSb/In0.53Ga0.47As source (>5×10^{19} cm^{-3}), a 6-nm-thick In0.7Ga0.3As pocket, a 150-nm-thick channel of In0.7Ga0.3As, and an In0.7Ga0.3As drain (>1×10^{18} cm^{-3}). Using a pocket layer next to the source can provide a remarkably small tunnel barrier and thus result in a remarkably high tunneling current. Fig. 1(b) and Fig. 2(b) show the band diagrams for the InGaAs homojunction TFET and the GaAsSb/InGaAs HTFET with a pocket. The effective tunnel barrier (Eb) in the InGaAs homojunction TFET is equal to an InGaAs bandgap of 0.74 eV. However, the Eb in the GaAsSb/InGaAs HTFET with a pocket is only 0.4 eV.

Device fabrication started with the deposition of Ti/Pt/Au (20/15/65 nm) metals to serve as a drain. Then drain metal with photoresist was used as an etching mask for etching down to the p+ GaAsSb source layer and H2PO4—H2O2 solution was applied to form the sidewall of the device. An ammonia solution (NH4OH—H2O) was used to clean the

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device surface before gate insulator deposition. An Al$_2$O$_3$/HfO$_2$ high-$k$ gate dielectric stack (1/5 nm) was deposited through atomic layer deposition at 150 °C. Postdeposition annealing was applied in N$_2$ ambiance at 300 °C for 1 min through RTA. Dry etching by SF$_6$, O$_2$, and Ar mixed gas was used for opening contact holes on the drain and source regions. Finally, Ni/Ti/Al/Ti/Au (30/25/650/35/100 nm) was deposited at the same time to serve as the source, gate, and pad. The gate metal was designed to be on the sidewall and the partial drain of the device. Fig. 3 shows the top view of the fabricated device and a cross-sectional view photographed through scanning electron microscopy along the cut-line. A small slope was produced in the side wall of the InGaAs homojunction TFET for gate metal deposition.

3. Experimental results and discussion

Fig. 4 shows the measurements of the $I_{DS}$–$V_{GS}$ transfer characteristics of the two TFETs at room temperature. At $V_{DS} = 0.5$ V and $V_{GS} = 2$ V, the maximum on-state current ($I_{ONMAX}$) was higher for the GaAsSb/InGaAs TFET with a pocket. The maximum on-state current for the HTFET with a pocket was 11.98 $\mu$A/µm, higher than the 0.19 $\mu$A/µm on-state current of the homojunction TFET. However, the off-state current was increased because of the reduced tunnel barrier. In addition, the $g_{m}$ of the GaAsSb/InGaAs HTFET with a pocket had a maximum value of 15.3 $\mu$S/µm.

Fig. 5 shows the measured $I_{DS}$–$V_{DS}$ output characteristics of the proposed GaAsSb/InGaAs HTFET with a pocket at room temperature. Its excellent output characteristics were demonstrated with a positive bias, and a negative differential resistance was observed with a negative bias. The $V_{DS}$ was increased from 0 V to 1.5 V, step = 0.5 V.
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