High sensitivity pH sensing on the BEOL of industrial FDSOI transistors

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A B S T R A C T

In this work we demonstrate the use of Fully Depleted Silicon On Insulator (FDSOI) transistors as pH sensors with a 23 nm silicon nitride sensing layer built in the Back-End-Of-Line (BEOL). The back end process to deposit the sensing layer and fabricate the electrical structures needed for testing is detailed. A series of tests employing different pH buffer solutions has been performed on transistors of different geometries, controlled via the back gate. The main findings show a shift of the drain current ($I_D$) as a function of the back gate voltage ($V_B$) when different pH buffer solutions are probed in the range of pH 6 to pH 8. This shift is observed at $V_B$ voltages swept from 0 V to 3 V, demonstrating the sensor operation at low voltage. A high sensitivity of up to 250 mV/pH unit (more than 4-fold larger than Nernstian response) is observed on FDSOI MOS transistors of 0.06 µm gate length and 0.08 µm gate width.

1. Introduction

Field effect transistor (FET) based sensors have been widely investigated due to their advantages of miniaturization, easy integration, label-free detection and direct transduction [1–3]. Ion Sensitive Field Effect Transistors (ISFET) were first proposed by Bergveld in 1970 [4], and have since found common applications as pH sensors. In ISFET devices, the metal gate electrode of the MOSFET is replaced with a chemically sensitive membrane, an electrolyte and a reference electrode. The ISFET pH sensor responds to surface potential changes caused by adsorption or desorption of hydrogen ions on the sensing membrane. It has been demonstrated that ISFET pH sensors can offer fast response, high sensitivity and high potential for integration into high volume production CMOS technology [1,2]. However, one of the disadvantages of such devices is the maximum sensitivity limit of 59 mV/pH (Nernst response) at room temperature. To improve the sensitivity beyond Nernst’s response, different architectures have been proposed, such as Dual Gate (DG) ISFET [5–7] with a thick bottom and thin front gate transistor structure acting as primary and secondary gate, respectively. The capacitive coupling thus created between the thick bottom and the thin front gates offers a high sensitivity that largely exceeds the limit of Nernst’s response. A detailed study on pH sensing using Silicon On Insulator (SOI) DG ISFET has been reported in [8], with a comparative study of pH response as a function of different oxide properties and channel thicknesses. The results identify high-k stacked membranes and thin Si channels as the optimal parameters to obtain high performance in SOI DG ISFETs. Another architecture based on ISFET has been proposed by Van der Spiegel et al. [9], named Extended Gate (EG) FET. This architecture offers better long-term stability with respect to classical ISFETs, as the structure separates the chemical environment from the gate insulator.

Fully Depleted Silicon on Insulator (FDSOI) MOSFETs have been demonstrated to operate with high speed at low voltages, low power consumption and good electrostatic channel control [10,11]. The intrinsic advantages of the FDSOI architecture can be extended to new applications and opportunities out of the scope of Moore’s Law. Monfray et al. [12] demonstrated the possibility of employing advanced FDSOI devices for sensing applications by using the back gate of the transistor as a control gate and the front
gate as a base for the sensing layer. The results show that a small charge variation on the front gate can induce a large shift of the back gate bias for the same drain current value. Thus this technology seems promising for sensing applications not only for its low cost and low power consumption, but also for the high sensitivity at low voltages.

This paper reports a proof of concept of using FDSOI MOS transistors as pH sensing devices with a sensing layer integrated in the BEOL, on top of the front gate, and using the back gate as a control gate. This is demonstrated through the fabrication and electrical testing of pH sensors based on STMicroelectronics industrial FDSOI MOSFET platform that can benefit from the high sensitivity at low voltages. This work focuses on a narrow range of pH between 6 and 8, as this is of interest for specific applications such as standard measurements of blood pH, that should vary around a value of 7 [13], and the pH measurement of sea water for environmental control [14].

The article is structured as follows: after the introduction in Section 1, Section 2 provides a detailed description of the concept of FDSOI MOSFETs used as pH sensors and the advantages brought by this specific technology. Section 3I details the back end process flow to fabricate the sensing layer and fan out the pads used for electrical tests. Section 4 is dedicated to the experimental details of the electrical tests on the MOS transistors under different pH conditions. Section 5, titled Results and discussion, details the experimental results of the electrical tests conducted on FDSOI MOSFET pH sensors with different geometries, when different pH buffer solutions are applied. Section 6 is dedicated to the main conclusions and future prospects to expand this work.

2. Concept of FDSOI MOS transistors as pH sensors

This study uses the STMicroelectronics NMOS FDSOI technology. It was demonstrated in [12] that advanced FDSOI transistors with ultra-thin Buried OXide (BOX) are more sensitive to any potential variation on the front gate compared to classical MOSFETs, where no back gate is available to sense it. Indeed the presence of a BOX allows better electrostatic control of the channel as compared to classical bulk MOSFETs.

Moreover, the front gate oxide is thinner than the BOX dielectric making the capacitive coupling of this top gate to the transistor channel larger than the back gate. Thus small potential variations on the front gate (used as gas sensing area) can induce a large back-gate threshold voltage shift. The use of FDSOI technology is therefore very promising for future generations of gas/pH sensors.

The transistor architecture, illustrated in Fig. 1, differs from bulk technology as the active layer is fabricated on an undoped Si layer of thickness $T_{Si}$. This layer is isolated from the substrate by a BOX of thickness $T_{BOX}$. It should be noted that a highly N doped NWELL is implanted under the BOX to form the back gate, which is part of the FDSOI CMOS process. A protection diode is connected to the gate stack to prevent the gate oxide from charging during the manufacturing process. As a consequence, there are two additional elements not featured in bulk transistors: the isolated undoped Si layer and the BOX. The NMOS transistors integrate a high-k HfO$_2$/TiN/poly-Si gate stack, with an electrical oxide thickness of $T_{ox} = 1.3$ nm, while $T_{Si} = 6$ nm and $T_{BOX} = 20$ nm. Vias are fabricated on top of the transistors to build aluminum pads for electrical tests, contacting the front and back gates, source, drain and protection diode.

To verify how a bias voltage (however generated) on the front gate can modulate the $I_D$ ($V_{G}$) characteristic (drain current $I_D$ as a function of the back gate voltage $V_{B}$), a test was run on a transistor of 0.02 $\mu$m length ($L$) and 0.06 $\mu$m width ($W$). The $I_D$ ($V_{G}$) characteristic is measured in dry air, at different front gate voltage values ($-0.1$ V, 0 V, and $+0.1$ V). Fig. 2 illustrates the three curves obtained, where the solid line is the characteristic at 0 V front gate bias. When a positive or a negative bias voltage ($0.1$ V or $-0.1$ V) are applied to the front gate, a large shift of the drain current ($I_D$) as a function of the back gate bias ($V_G$) is observed respectively to the left or right. For example, at $I_D = 1 \times 10^{-6}$ A, a shift of $-110$ mV (at 0.1 V) and $100$ mV (at $-0.1$ V) is observed compared to the characteristic measured at 0 V on the front gate. This demonstrates the capability of the transistor to detect a voltage bias on the front gate through a high modulation of the back gate threshold voltage.

Before testing the FDSOI sensor under pH buffer solutions, a series of back end process steps are needed in order to fan out the pads for the source, drain, back gate and protection diode. An adequate sensing layer material must be selected and the back end designed to account for a chip area dedicated to pH droplet tests. The selection of the sensing layer material is an important parameter to enable a good interaction with pH buffer solutions. In the literature different thin films used as a sensing material in pH FETs have been studied, such as carbon nanotubes [15], SnO$_2$ [16], and ZnO [17]. Among the studied materials, however, silicon nitride ($Si_3N_4$) deposited in thin layers is one of the most investigated [18,19]. Several research groups have demonstrated $Si_3N_4$ to react with buffer solutions of different pH values by adsorption or desorption of hydrogen ions on the sensing surface. For the purposes of this work, silicon nitride is selected as the sensitive layer as it is a well-established sensing material and it is compatible with CMOS manufacturing.

The performance of FDSOI MOS transistors as pH sensors is tested as follows: (a) a pH buffer solution is applied to the sensing

**Fig. 1.** Diagram of a MOS transistor: NWELL in light blue, silicon dioxide layers in yellow, gate stack in light orange, depleted channel in light blue, source and drain implants in purple, aluminum vias in black.

**Fig. 2.** Drain current ($I_D$) as a function of the back gate bias ($V_B$) for an NMOS FDSOI transistor operating in the linear regime ($V_G = 0.1$ V) for three different gate front gate bias values ($-0.1$ V, 0 V, 0.1 V). The transistor dimensions are $L = 0.02 \mu$m and $W = 0.06 \mu$m.
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