New modeling method for the dielectric relaxation of a DRAM cell capacitor

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ABSTRACT

This study proposes a new method for automatically synthesizing the equivalent circuit of the dielectric relaxation (DR) characteristic in dynamic random access memory (DRAM) without frequency dependent capacitance measurement. Charge loss due to DR can be observed by a voltage drop at the storage node and this phenomenon can be analyzed by an equivalent circuit. The Havriljak-Negami model is used to accurately determine the electrical characteristic parameters of an equivalent circuit. The DRAM sensing operation is performed in HSPICE simulations to verify this new method. The simulation demonstrates that the storage node voltage drop resulting from DR and the reduction in the sensing voltage margin, which has a critical impact on DRAM read operation, can be accurately estimated using this new method.

1. Introduction

To maintain a sufficient sensing margin in dynamic random access memory (DRAM) operation, the storage capacitance value should be as large as possible to overcome the scaling of memory cell area [1]. Because the scaling of the DRAM cell capacitor with a SiO2 dielectric has been adopted to utilize a thicker equivalent oxide [2]. However, the dielectric relaxation (DR) current in high-k dielectrics has been found to be related to the degree of polarization [4]. When a dielectric is placed in an electric field, dielectric polarization occurs. This phenomenon creates an internal electric field that reduces the overall field in the dielectric. After the sudden removal of the initial polarizing field, the polarization begins to decay. This decay is generally referred to as DR [5]. Moreover, various mathematic models for describing the DR characteristic have been introduced [4–7].

In DRAM operation, the effect of DR during the retention time was explained by quick and slow response capacitors [3]. Because the charge in the slow response capacitor cannot respond during the nanosecond scale sensing period, the DR effect is important for accurately estimating the sensing voltage margin. The DR effect can be modeled by the equivalent circuits proposed in [8–10]. However, the literature has not investigated how to synthesize the DR equivalent circuit by extracting the parameter from mathematic models. Moreover, the majority of studies have extracted DR characteristics from capacitance-frequency (C-f) or current–time (I-t) measurements [3–4,8–16]. Due to large parasitic effects, C-f measurements within the high frequency range require a de-embedding technique that eliminates the parasitic components of test patterns. However, this technique is extremely difficult to carry out with real DRAM structure, which is an array structure with multiple connected cells. In contrast, storage node voltage-time (Vsn-t) measurements on DRAM chips can be conducted without parasitic effects.

This paper presents a new method for synthesizing an equivalent circuit for the DR characteristic. To realizing equivalent circuit of DR, we extract the parameters of the DR using Vsn-t characteristics instead of C-f measurements. Using this method, the capacitance-time (C-t) and C-f characteristics can be obtained from Vsn-t. Moreover, the equivalent circuit modeling accuracy is improved by an applying appropriate mathematic model of the DR. The remainder of this paper is organized as follows. First, the procedure for synthesizing an equivalent circuit for a DR capacitor is introduced. Then, mathematic models for explaining DR behavior are discussed. After realizing the equivalent circuit of DR, we apply it to DRAM operation simulations to analyze the influence of DR on DRAM operation.

2. Simulation method

A DRAM cell capacitor is described by an equivalent parallel circuit of an intrinsic capacitor and a component describing the DR [8–10]. As shown in Fig. 1(d), the intrinsic capacitor responds rapidly to a change in the applied voltage, whereas the DR capacitor part responds slowly to a change in the applied voltage. The DR capacitor part consists of parallel RCs with different relaxation times (τ).
In DRAM operation, the charge is stored in the quick response capacitor because the write operation is accomplished in a short time. Until the next read operation, the charge in this quick response capacitor moves toward slow response capacitors. Each parallel RC responds when the charge in slow response capacitors cannot respond during the short read time. Therefore, it is important to investigate the DR characteristic because only the charge of the quick response capacitor can contribute to the bit line voltage during the read operation.

The majority of studies have extracted DR characteristics from the C-f measurement [4,13-16]. However, an accurate capacitance measurement at a high frequency in the range of DRAM operation speed is extremely difficult in a real DRAM structure. Therefore, instead of the C-f measurement, we analyze the DR characteristic using the storage node voltage \( V_{\text{sn}} \), which was obtained by conducting electrical tests on the main DRAM chip. Fig. 1 shows the procedure for realizing the equivalent circuit. The value of \( V_{\text{sn}} \) is the related dielectric permittivity, \( g_A \) is the integral value of the relaxation time distribution function of the CS relaxation model \[\langle g_{cs}(t) \rangle \), and \( \Delta t_k \), and \( A \) and \( d \) are the area and thickness of the capacitor, respectively.

Table 1 Parameters used in this paper.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_0 )</td>
<td>5 fF</td>
<td>Initial capacitance (= quick response capacitance)</td>
</tr>
<tr>
<td>( V_d )</td>
<td>1.15 V</td>
<td>Initial storage node voltage</td>
</tr>
<tr>
<td>( \alpha )</td>
<td>0.9924</td>
<td>CS model parameter</td>
</tr>
<tr>
<td>( C_{DR} )</td>
<td>5.7721 fF</td>
<td>CS model parameter</td>
</tr>
<tr>
<td>( \Delta t_k )</td>
<td>0.2 decade</td>
<td>Time interval of the distribution function</td>
</tr>
<tr>
<td>( \beta )</td>
<td>0.18</td>
<td>HN model parameter</td>
</tr>
<tr>
<td>( \tau_{0n} )</td>
<td>( 10^{-7} ) s</td>
<td>HN model parameter</td>
</tr>
</tbody>
</table>

Using Eq. (1), which is obtained by the CS relaxation model [17].

\[
C(f) = C_0 + C_{DSR} \sin \left( \frac{n \pi}{2} \right) (2\pi)^{n-1} f^{n-1} \quad (0 < n < 1), \tag{1}
\]

where \( C_{DSR} \) is the high frequency limit of capacitance and parameters \( n \) and \( C_{DSR} \) are extracted to determine the equivalent circuit. The value of \( n \) indicates the degree of DR and determines the slope of \( C-f \) [4].

The kth R and C of the equivalent circuit \( (R_k \) and \( C_k ) \) are extracted from the C-f characteristics using a mathematical model. Various mathematical models exist for describing the characteristics of DR [4-7]. Because the general type of DR can be described by the Curie-von Schweidler (CS) model [4], we first tried to fit the C-f characteristic using Eq. (1), which is obtained by the CS relaxation model [17].
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