Int. J. Production Economics 130 (2011) 96–103

Contents lists available at ScienceDirect

Int. J. Production Economics

journal homepage: www.elsevier.com/locate/ijpe

Reliability deployment in distributed manufacturing chains via closed-loop Six Sigma methodology

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ARTICLE INFO

Article history:
Received 22 June 2009
Accepted 19 November 2010
Available online 24 November 2010

Keywords:
Six Sigma program
Reliability growth
Distributed supply chain
Subcontract manufacturing
Capital equipment

ABSTRACT

This paper proposes a Six Sigma based framework to deploy high product reliability commitment in distributed subcontractor manufacturing processes. The study aims to expand the Six Sigma tools in applications, where products are designed and developed under the fast time-to-market requirement. The reliability deployment is driven by two incentives: the customer satisfaction and the reduction of the warranty cost. A closed-loop control mechanism is created between the upper and the lower manufacturing streams to identify and remove the early life failures occurred during the initial system installation. A cross-functional team is formed to implement Six Sigma tools for resolving critical failures arising in the upper manufacturing stream. The ultimate goal is to achieve high product reliability in the shortest time when the product time-to-market is essential for gaining the market share. Finally, the proposed control mechanism is demonstrated on the system designs drawn from the semiconductor testing industry.

1. Introduction

In semiconductor, telecommunication and other technology-driven industries, the requirements of highly-reliable products render traditional reliability methods obsolete due to the shrink of the design cycle. The situation becomes more challenging as these industries are shifting to the distributed manufacturing paradigm. The distributed manufacturing paradigm is built upon a pipeline, where the customer demands pushes the design, the design drives the manufacturing, and the manufacturing further pushes the final shipment. Given such a compressed design cycle, it is almost impossible for equipment manufacturers to implement extended in-house reliability growth testing. While the new paradigm may shrink the design cycle and reduce the manufacturing cost, if not properly managed, the manufacturer may incur escalated warranty costs and receive excessive customer complaints due to the poor product reliability. Eventually it may result in the long term damage to the market share and the credibility. Fig. 1 depicts the life cycle of automatic test equipment (ATE) from the design to the field deployment in the distributed manufacturing paradigm. ATE is a high-end electronics system widely used for testing wafers and devices in semiconductor industry.

In the last two decades, many companies, such as Motorola, General Electric (GE), and Raytheon, have embraced the Six Sigma program to improve customer satisfaction, product quality, and reliability (Treichler et al., 2002). Yu and Yu (2007) formulate an optimization program to optimize the mixed policy of inspection and burn-in time to maximize the expected profit while satisfying the reliability and average outgoing quality of products. As pointed out by De Feo and Barnard (2005) about two-thirds of the Fortune 500 organizations have begun Six Sigma initiatives with the aim of reducing costs and improving quality by the late 1990s. The implementation of Six Sigma positively impacts many Critical-to-Quality (CTQ) measures: timeliness/speed, cost, quality of product/service, and customer satisfaction.

These benefits usually are achieved through the utilization of a systematic step-wise approach, the DMAIC process (Define, Measure, Analyze, Improve, and Control). Six Sigma projects stay on track by establishing deliverables at each phase of the DMAIC process. One of the advantages of Six Sigma methodology over other improvement programs is that it enables practitioners to accurately remove hindering issues and demonstrate the improvements using statistical tools such as Pareto Chart and control charts (Kapur and Feng, 2005; Feng and Manuel, 2008).

To simultaneously deliver new designs in a timely fashion with high reliability, this paper aims to propose a reliability deployment framework by proposing a closed-loop Six Sigma model. In particular, our study intends to expand the Six Sigma applications, where products are designed under the fast time-to-market requirement.

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doi:10.1016/j.ijpe.2010.11.020

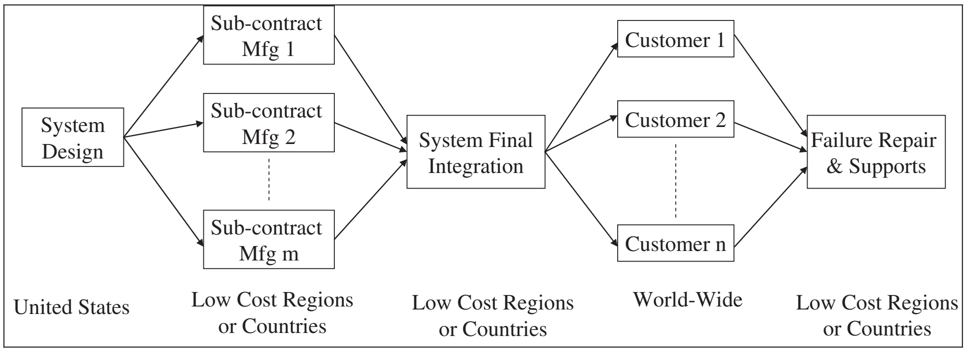

Fig. 1. ATE life cycle in the distributed manufacturing environment.

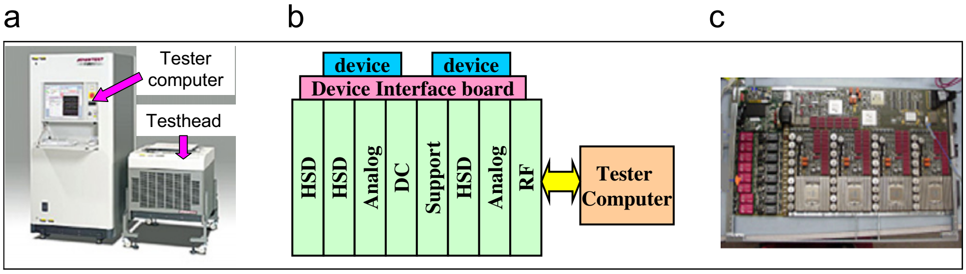

Fig. 2. (a) An actual ATE system; (b) a generic ATE testhead and (c) a PCB module.

Our method is devised for and will be implemented in the electronics testing equipment industry, where the product development cycle is typically six to nine months. We approach the distributed supply chain from two perspectives: (1) improve external customer satisfactions; and (2) reduce the internal operational budget such as warranty costs. The proposed method will be a customer-focused, data-driven and robust methodology across the product life cycle (Yang and El-Haik, 2003; Shah et al., 2008; Bunce et al., 2008).

The rest of the paper is organized as follows. In Section 2, two grand challenges in ATE supply chain will be discussed. Section 3 introduces the closed-loop reliability deployment mechanism across the distributed supply chain using the Six Sigma methodology. In Section 4, an illustrative example drawn from the semiconductor equipment industry is used to demonstrate the effectiveness of the methodology. Section 5 summarizes the paper with some remarks on the future research.

2. Challenges in distributed supply chain

ATE is widely used to perform device functional and parametric tests at the back-end of the semiconductor manufacturing process. It is a capital intensive system and typically costs $1–3 million depending on the equipment performance. An unscheduled equipment downtime lasting one hour could cause significant amounts of production loss.

The major part of the system (see Fig. 2(a)) is the testhead, where multiple instrument modules made by printed circuit boards (PCBs) are populated in order to generate the desired testing signals. Fig. 2(b) depicts an ATE testhead configured with eight PCB modules to test two devices simultaneously. Depending on the performance and functionality, the price for an individual instrument module (see Fig. 2(c)) ranges from $40,000 to $100,000. The device interface board provides electrical connections between the instrument modules and the device under test.

The distributed manufacturing paradigm poses grand challenges in designing and producing high-end electronics systems. Product quality becomes more vulnerable and easier to be infiltrated by various types of defects arising from product design, manufacturing process, system integration, and field deployment. A significant portion of these defects manifested as reproducible failures are caused by defective hardware components, design weakness, software bugs, manufacturing faults, and process-related issues. Although systems are designed with certain protection mechanisms such as current fuses or voltage guard bands, unpredictable operational profiles or human errors could still breach the protection barrier and lead to field failures in the customer sites.

2.1. *Compressed design cycle*

The rapid advancement of technology usually renders electronics systems, especially semiconductor testing equipment, obsolete every five to seven years. Hence a new design must be transformed into a competitive yet reliable product in a timely manner. A common practice used by electronics equipment manufacturers is to adopt the asynchronous development strategy so that new designs can be delivered to customers in a timely manner.

Fig. 3 shows a typical design cycle for a new testing system developed under an asynchronous fashion. The equipment manufacturer begins to deliver the new system at time t_1 right after the completion of the basic instrument modules. Meanwhile, advanced modules such as 4, 5 and 6 are still in the design or even concept phase. Later on, customers, after purchasing the basic system, have the flexibility to upgrade the existing configuration by installing advanced modules. In such a compressed design schedule, priorities are often given to the system functionality rather than the reliability. Many times system reliability growth is achieved through rigorous corrective actions after the volume shipment.