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The ATLAS Planar Pixel Sensor R&D project

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ABSTRACT

Within the R&D project on Planar Pixel Sensor Technology for the ATLAS inner detector upgrade, the use of planar pixel sensors for highest fluences as well as large area silicon detectors is investigated. The main research goals are optimizing the signal size after irradiations, reducing the inactive sensor edges, adjusting the readout electronics to the radiation induced decrease of the signal sizes, and reducing the production costs.

Planar n-in-p sensors have been irradiated with neutrons and protons up to fluences of $2 \times 10^{16}\,n_{eq}/cm^2$ and $1 \times 10^{16}\,n_{eq}/cm^2$, respectively, to study the collected charge as a function of the irradiation dose received. Furthermore comparisons of irradiated standard 300 μm and thin 140 μm sensors will be presented showing an increase of signal sizes after irradiation in thin sensors. Tuning studies of the present ATLAS front end electronics show possibilities to decrease the discriminator threshold of the present FE-I3 read out chips to less than 1500 electrons.

In the present pixel detector upgrade scenarios a flat stave design for the innermost layers requires reduced inactive areas at the sensor edges to ensure low geometric inefficiencies. Investigations towards achieving slim edges presented here show possibilities to reduce the width of the inactive area to less than 500 μm.

Furthermore, a brief overview of present simulation activities within the Planar Pixel R&D project is given.

1. Upgrade challenges

The present pixel detector of the ATLAS experiment constitutes the innermost part of the tracking system. Distributed on three barrel layers at radii between 50.5 and 122.5 mm and six discs a total of 1744 pixel modules are mounted allowing for a three hit track reconstruction of charged secondary particles [1]. Each module contains a 250 μm thick large scale n-in-n pixel sensor of $62.6 \times 18.6\,mm^2$ with pixel implants of $50 \times 400\,\mu m^2$. Connected to each sensor are 16 $7.4 \times 11.0\,mm^2$ ATLAS FE-I3 [2] chips with a total of 46 080 readout channels. Both the sensors and the electronics of the present ATLAS pixel modules are specified to work up to a fluence of $10^{15}\,n_{eq}/cm^2$ (1 MeV neutrons).

While the nominal luminosity of the present LHC accelerator is $10^{34}\,cm^{-2}/s$, an upgrade to increase the luminosity by a factor of 10 is planned to be carried out in a two phase process [3]. In *Phase* 1 an upgrade to $(2-3) \times 10^{34}\,cm^{-2}/s$ is foreseen without any changes to the machine hardware up to the year 2014. The *Phase* 2 upgrade to the Super LHC (SLHC) around 2018 is expected to reach a maximum luminosity of $10^{35}\,cm^{-2}/s$ with modifications to the insertion quadrupoles and changes in the main machine parameters. In this scenario the innermost layer of the ATLAS pixel system will have to sustain fluences reaching $(3-4) \times 10^{15}\,n_{eq}/cm^2$ during the *Phase* 1 upgrade and $(1-2) \times 10^{16}\,n_{eq}/cm^2$ during the SLHC running period [4]. The resulting defects in the semiconductor sensors cause high leakage currents and a reduced charge collection distance. Consequently it will be a challenge to develop semiconductor sensors that will yield a sufficient signal to noise ratio.

In addition the luminosity upgrades will lead to an increase of the occupancy of the detector components. Reducing the pixel size in the inner part of the tracking detectors is a natural choice for decreasing the occupancy and at the same time increasing the spatial resolution. Succeeding the FE-I3 readout chip, the $20.0 \times 18.6\,mm^2$ FE-I4 chip [5] will feature a reduced pixel size of $50 \times 250\,\mu m^2$ to address these issues. Consequently, it might be beneficial to extend the current pixel detector with additional layers to larger radii replacing parts of the silicon strip detector. This would allow to decrease the occupancy at these radii while further increasing the track resolution. To realize such large scale pixel detectors the production costs have to be minimized.

While a complete replacement of the ATLAS tracking system is planned for the *Phase* 2 upgrade only a newly designed *b-layer*

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is planned to be inserted into the present innermost pixel layer for the first phase. This is achieved by using a beam pipe of reduced radius and a very compact new pixel module to efficiently populate the given volume. Due to space limitations and restrictions on the material budget the new pixel modules will have to be mounted on *flat staves*. Overlaps of modules in the direction of the beam pipe will not be possible. To stay below the target geometric inefficiency of less than 2.5% it is mandatory to reduce the inactive areas around the pixel implants to less than 500 μm [6]. Similar restrictions might likely also apply to the innermost layers of the pixel detector for a future *Phase* 2 luminosity upgrade.

Different detector concepts are being developed in several research activities to address the challenges imposed by the foreseen luminosity upgrades. They include pixel sensors made of diamond [7] and sensors with three-dimensional implants lancing through the silicon bulk [8]. Optimizing the well-known technology of planar silicon pixel sensors for the ATLAS detector at an upgraded LHC accelerator is carried out within the Planar Pixel Sensor project.

2. The Planar Pixel Sensor project

Planar pixel sensors are the present standard technology for tracking detectors in high energy physics. Much experience of designing, optimizing, and producing silicon sensors has been accumulated and progress towards further improvements is ongoing. Many industrial suppliers and research laboratories are able to produce considerable quantities of relatively low cost and high yield planar sensors. Hence, planar sensors are investigated for upcoming generations of tracking detectors at particle accelerators.

The Planar Pixel Sensor (PPS) project is a collaboration of 16 European, American, and Asian groups investigating the possibilities to meet the aforementioned challenges of radiation hardness, low cost production, and reducing inactive edges of planar silicon sensors.

2.1. Radiation hardness

To achieve a sufficient signal to noise ratio after highest irradiations, various planar sensor technologies are being compared. These include different bulk dopings, i.e. the standard n-in-n and the alternative n-in-p sensor design which has become a competing choice since sensor grade wafers are procurable. Standard n-in-n sensors need to have patterned guard ring structures on both sides of the sensors since the bulk type is inverted during irradiations. In contrast, the non-inverting p-type bulk allows for having only a homogeneous implant on the high voltage back side. This considerably decreases the production costs compared to structured implants. On the other hand the drop between the high voltage applied to the back side and the readout electronics potential (~ 0 V) occurs solely on the sensor top side facing the readout electronics. Hence the risk of sparks is investigated within the R&D work.

In addition to the different bulk dopings also various silicon materials are compared for their radiation tolerance. These include crystals grown by Float Zone, Magnetic Czochralski, and Epitaxial techniques. Also reduced sensor bulk thicknesses are studied since they allow for a lower material budget as well as higher electric fields. While the former reduces multiple scattering the latter might be beneficial for the charge collection efficiency after highest irradiations.

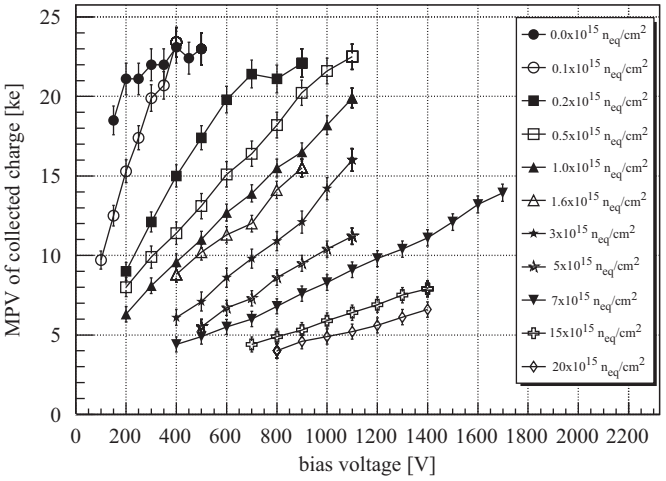

Fig. 1. Most probable values for the collected charge after different neutron fluences for different bias voltages [9].

2.2. Low cost large area pixel detectors

Pixel detectors offer a better spatial and 2-track resolution than other detector systems. The size of the area that can be equipped with pixel sensors mainly depends on the cost per area. For the present ATLAS pixel detector this was dominated by the cost of the bump bonding process to connect sensors and readout chips. To reduce the cost new low-cost flip-chipping technologies are evaluated. These include the C4NP solder technology by Süss/IBM, anisotropically conductive glues and tape-assisted bonding. Furthermore, possibilities for a cost reduction of the presently used bump bonding technology by IZM[1] are being investigated.

2.3. Reduction of inactive sensor edges

As shingling, i.e. overlapping of pixel modules in the direction of the beam pipe is not possible in the innermost areas of upgraded ATLAS pixel detectors, the possibilities of reducing the inactive areas at the edges of the sensors are studied. This is done by optimizing the dimensions of the guard ring structures and reducing the safety margins between the outermost guard ring and the cutting edge.

3. Characteristics of n-in-p sensors after SLHC fluences

To study the signal sizes of irradiated planar pixel sensors first charge collection measurements were carried out on n-in-p strip sensors after neutron and proton irradiations [9,10]. The sensors with a thickness of 300 μm were produced by Micron[2] and contain a total of 128 strips with a strip length of 1 cm and an 80 μm pitch. Irradiations with neutrons to fluences reaching $2\times 10^{16}\,n_{eq}/cm^2$ were performed at the TRIGA Mark II research reactor in Ljubljana. Proton irradiations up to $1\times 10^{16}\,n_{eq}/cm^2$ were done at the CERN-PS Irrad1 facility at a momentum of 24 GeV/c and at the Compact Cyclotron in Karlsruhe with a kinetic energy of 26 MeV/c^2.

Figs. 1 and 2 show the most probable value of the collected charges generated by minimum ionizing particles, measured with an analogue 40 MHz readout system based on the SCT128a chip as functions of the applied bias voltage. The temperatures of the

[1] Fraunhofer-Institut für Zuverlässigkeit und Mikrointegration, IZM, http://www.izm-m.fraunhofer.de

[2] Micron Semiconductor Ltd., http://www.micronsemiconductor.co.uk