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Modeling semiconductor testing job scheduling and dynamic testing machine configuration

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Abstract

The overall flow of the final test of integrated circuits can be represented by the job shop model with limited simultaneous multiple resources in which various product mixes, jobs recirculation, uncertain arrival of jobs, and unstable processing times complicate the problem. Rather than relying on domain experts, this study aims to develop a hybrid approach including a mathematical programming model to optimize the testing job scheduling and an algorithm to specify the machine configuration of each job and allocate specific resources. Furthermore, a genetic algorithm is also developed to solve the problem in a short time for implementation. The results of detailed scheduling can be graphically represented as timetables of testing resources in Gantt charts. The empirical results demonstrated viability of the proposed approach.

Keywords: Semiconductor final testing; Machine configuration; Timetabling; Genetic algorithm; Intelligent manufacturing; Scheduling

1. Introduction

The semiconductor industry has grown rapidly and subsequent production planning problems have raised many important research issues (Lee, Uzsoy, & Martin-Vega, 1992; Leachman, 1993). The semiconductor companies compete with each other in cost structure, quality, and the delivery to maintain their competitive advantages (Chien, Wang, & Cheng, 2007). The semiconductor manufacturing scheduling problem is complicated by various product mixes, jobs recirculation, uncertain arrival of jobs, and unstable processing times. In particular, final testing of integrated circuits (IC) devices is the final operation in semiconductor manufacturing. The objectives of final test are to deliver passed IC devices of the required quality on time to customers while using resources efficiently. The overall flow of the final test can be represented by the job shop model with limited resources. Many optimization models or algorithms for short-term production planning at the shop floor level have been developed. However, the manufacturing environment of final test is unstable and uncertain. For example, the machine condition is uncertain affecting the yield rate and the throughput. Hence, the scheduling problem of final test is more complex than the conventional job shop scheduling problem. The testing site is typically the bottleneck of the final test operation because the equipment at the testing site is expensive and limited in amount. Also, final test directly suffers from the uncertain arrival of jobs from upstream, job recirculations, long job processing time, and long machine setup time. Engineers who rely on personal domain knowledge cannot find optimal machine configuration to respond to production needs rapidly and effectively. However, few studies have been done to address the present problem.

Focusing on real settings, this study aims to develop a hybrid approach to address semiconductor final test scheduling problem (SFTSP). In particular, the following manufacturing characteristics are considered. Firstly, the machines in the semiconductor final test facility are indeed

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the combinations of specific testers, handlers, and accessories. Such resources are limited and scheduling approaches must take the resource constraint into account (Chen, Chang, Chen, & Kao, 1995; Chien & Chen, 2007a). Secondly, while different types of test machines (different combinations of resources) can process the test for a given product at different speeds (different utilization rates), one machine configuration may be able to perform tests on more than one type of products. In addition to determine the testing schedule, the problem assigning a specific test machine configuration to a test job, given the limited resources, remains. Thirdly, changeover between different machine configurations requires sequence-dependent setup time including the disassembly time for original configurations and the assembly time for new machine configurations. Certainly, the sequence-dependent setup time reduces the utilization of testing resources and a good schedule avoids unnecessary setups (Chien & Chen, 2007b). Fourthly, the recirculations of testing jobs should be considered to ensure practical viability of the proposed scheduling method (Chien & Wu, 2003). Fifthly, some jobs that are released late but with higher priority and should be delivered on time may interrupt the earlier schedule. Consequently, developing consistently well-performed algorithms for scheduling testing jobs is difficult. In this study, we developed a mathematical programming model to optimize the testing job scheduling and proposed an algorithm to specify the machine configuration of each job and allocate specific resources. Furthermore, a genetic algorithm is also developed to solve the problem in a short time for practical viability. The results of detailed scheduling can be graphically represented as timetables of testing resources in Gantt charts. For validation, the results of the proposed approach are then compared with those of existing models.

The rest of this paper is organized as follows. Section 2 structures the semiconductor final test scheduling problem and reviews related research. Section 3 presents a mathematical model of job scheduling and the assignment algorithm to determine the machine configuration. Section 4 proposes a genetic algorithm to solve this problem. Section 5 compares the experimental results of the proposed model and genetic algorithm with those of existing studies. Conclusions and future research suggestions are finally made in Section 6.

2. Semiconductor final test and relative scheduling problems

The final test of IC devices is generally divided into the operations of Functional Test, Burn-in, Scan, Bake, Tape and Reel Station, and Package and Load Station. The Test site is the main operation site of the final test process and includes Room Test, Hot Test, and Cold test. The IC functional test is performed with testers, handlers, and accessories. Specific products can be tested only with appropriate machine configurations of testers, the handlers, and accessories. The tester, a central processing unit, loads test programs and is connected to the packaged IC devices via test heads to test their functions. Handlers, with built-in temperature control systems that enable tests in various temperatures, use suitable material handling devices called boats to load ICs by lots that packed in plastic antistatic trays or tubes. The boats release ICs from the trays or tubes and the suction devices (called nests) lift and load the ICs onto an electrical interface (called the load board) between the packaged circuits and the tester. After the functional test, the tested ICs are automatically removed from the handler and placed into the classified trays (or tubes) according to the results (i.e., passed or failed). The board and the nest are called the accessory (or kit). The jobs considered in the SFTSP are the IC devices in lots that were released from on-hand WIP or the output forecast of the assembly (i.e., the preceding operation to final test).

However, the machine configuration may not always be fixed. Different products can be tested by specific machine configurations (i.e., the corresponding combinations of testers, handlers, and accessories) with different processing times. It requires sequence-dependent setup time (SDST) to disassemble the original machine and assemble the new machine to test a different product. The quantities of testing resources such as testers, handlers, and accessories available in a final test facility are determined by long-term capacity planning. However, the daily availabilities of the resources are time-dependent and are influenced by the factors including current product-mix, equipment maintenance, machine breakdowns, and ongoing R&D experiments. Certain lots of IC devices would undergo functional testing more than once (i.e., recirculation). Thus, schedulers should trace the recirculated jobs and retain some machine capacity for them, which complicates the SFTSP. The present problem is to determine a testing job schedule and allocate appropriate combinations of resources to conduct the corresponding testing jobs.

A number of studies have been done on scheduling for semiconductor final test facilities. For example, Uzsoy, Martin-Vega, Lee, and Leonard (1991) and Ovacik and Uzsoy (1996) modeled and scheduled SFTSP including sequence-dependent setup time (SDST) based on the well-known shifting bottleneck approach developed by Adams, Balas, and Zawack (1988). After a number of computational experiments, they concluded proposed approaches significantly outperforming contemporary methods and CPU times being reasonable. The proposed decomposition methods were suggested applicable to SFTSP as well as the conventional job shop problems. Freed and Leachman (1999) further examined the multihead multiple tester scheduling problem where the head interdependency was taken into account and thus presented an enumerative solution technique. However, utilizing the contemporary tester scheduling methods for the multihead multiple test scheduling problems could result in infeasible or inferior solutions. In addition, Chien and Chen (2007b) developed a batch sequencing genetic algorithm embedded with a novel timetabling algorithm to solve the scheduling