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Hybrid data mining approach for pattern extraction from wafer bin map to improve yield in semiconductor manufacturing

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Abstract

Semiconductor manufacturing involves lengthy and complex processes, and hence is capital intensive. Companies compete with each other by continuously employing new technologies, increasing yield, and reducing costs. Yield improvement is increasingly important as advanced fabrication technologies are complicated and interrelated. In particular, wafer bin maps (WBM) that present specific failure patterns provide crucial information to track the process problems in semiconductor manufacturing, yet most fabrication facility (fabs) rely on experienced engineers' judgments of the map patterns through eye-ball analysis. Thus, existing studies are subjective, time consuming, and are also restricted by the capability of human recognition. This study proposes a hybrid data mining approach that integrates spatial statistics and adaptive resonance theory neural networks to quickly extract patterns from WBM and associate with manufacturing defects. An empirical study of WBM clustering was conducted in a fab for validation. The results showed practical viability of the proposed approach and now an expert system embedded with the developed algorithm has been implemented in a fab in Taiwan. This study concludes with a discussion on further research.

Keywords: Data mining; Yield improvement; Wafer bin map; Spatial randomness test; ART1; Neural networks; Semiconductor manufacturing; Quality engineering

1. Introduction

The semiconductor manufacturing processes are lengthy and complex. Thus, the capital investments in the semiconductor industry are huge. The manufacturing usually contains 100–200 process steps, in which the wafers move from step to step in groups of 25 or 24 identical wafers in a fabrication facility (fab). After wafer fabrication, circuit probe (CP) testing is performed on each die on the wafer. Then, the wafers are died up, and the good dies are packaged into chips and shipped to the customer after final testing (FT).

The critical factors maintaining competitive advantages for semiconductor wafer fabs include lowering die costs via lean production and increasing yield via quick response to yield excursions (Leachman and Hodges, 1996; Peng and Chien, 2003). In particular, the defect problems should be detected in time and the assignable causes should then be resolved to reduce the loss of hundreds of thousands of dollars of scraped wafers as soon as

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possible. Four yield definitions are used in semiconductor manufacturing: CP test yield (CP yield, Y_{CP}), fabrication line yield (Y_L), assembly yield (Y_{AS}) and final test yield (Y_{FT}). Among them, the CP yield is the most critical (Cunningham et al., 1995). CP yield improvement is divided into two major categories: (1) based line yield improvement, and (2) low yield trouble shooting. The based line yield improvement is based on tuning the process recipes to improve device performance and reduce defects, while low yield trouble shooting involves monitoring and diagnosing the failures caused by abnormal events such as mis-operation, trouble tool and contamination. Wafer bin map (WBM) is the result of CP inspection of dies on the wafer at the end of fabrication. WBM patterns can provide information to monitor the process and product.

This study aims to develop a hybrid data mining approach that integrates spatial statistics and adaptive resonance theory (ART) neural networks to rapidly extract patterns from WBM and associate them with manufacturing defects. An empirical study of WBM clustering was conducted in a fab for validation. Mining large amounts of data can help the engineers make the right decision of classifying patterns. During the manufacturing process, data are collected for various purposes. In particular, Wafer In Process (WIP) data refers to the data collected while processing wafers; metrology data refers to the data collected from in-line inspections; electrical test (E-test) data refers to data collected to measure device performance in chips, and the CP test data records each chip' functional test result after wafer fabrication. Since modern fabs are equipped with the computer integrated manufacturing (CIM) system, data collection is no longer a major issue. Furthermore, an engineering data analysis (EDA) system that is an off-line analysis-oriented system with data warehouse is generally developed to support data analysis activities (Peng and Chien, 2003; Chien et al., 2007). A remaining issue is to sieve out relevant data from a massive pool to derived useful information that can assist engineers in timely trouble shooting and yield enhancement.

WBMs are multi-dimensional and have complex structures, can provide essential information for engineers to identify problems in the manufacturing process. Fig. 1 shows a typical WBM where the different symbols denote chips failing in different functional tests. To assist visualization and analysis, WBM is usually transformed into a binary map that represents it using binary code or two different colors. This study uses yellow squares or "1" to denote defective chips, and red squares or "0" to denote functional chips.

The failure patterns of WBM can be classified into three major categories (Taam and Hamada, 1993; Stapper, 2000):

(1) Random defect: No spatial clustering or pattern exists, and the defective chips are randomly distributed in the two-dimensional map. Random defects are usually caused by the manufacturing environmental factors. Even in a in a near-sterile environment, particles cannot be removed completely. However, reducing the level of random defects can improve the overall productivity of wafer fabrication.
(2) Systematic defect: The positions of defective chips in the wafer show the spatial correlation, for example, ring, edge-fail, checkerboard. Fig. 2 shows 10 systematic patterns that are frequently seen in fab, as defined by domain experts.

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a
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        %%* * S a d d %* S
     m%w%mmm%%%G%* %
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%%* * S %%%* * * * I * * * %* *
* S * %%%* %%%%* * * d * %* *
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* * * %%* * * %* %%* * G* s * *
     %%* * %* * f * * %* * %* *
       * * %* * * * %* * * * %*
          * * * d %* * * * * %*
```

```
b
          * * %* * * * *
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          * * * * %* * * * %*
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Fig. 1. Example of WBM: (a) WBM with each failure bin denoted by a different symbol; (b) WBM with specific bin denoted by the symbol "%".