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Development of a soldering quality classifier system using a hybrid data mining approach

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ABSTRACT

Soldering failures lead to considerable manufacturing costs in the electronics assembly industry. Soldering problems can be caused by improper parameter settings during paste stencil printing, component placement, the solder reflow process or combinations thereof in surface mount assembly (SMA). Data mining has emerged as one of the most dynamic fields in processing large manufacturing databases and process knowledge extraction. In this study, the integration of a probabilistic network of the SMA line and a hybrid data mining approach is employed to identify soldering defect patterns, classify soldering quality, and predict new instances according to significant process inputs. The hybrid data mining approach uses a two-stage clustering method that utilizes the self-organizing map (SOM) to derive the preliminary number of clusters and their centroids from the statistical process control (SPC) database, followed by the use of K-means to precisely classify instances into definite classes of soldering quality. The See5 induction system is then applied to induce the decision tree and ruleset to elucidate associations among the defect patterns, process parameters, and assembly yield. Finally, visual C++ programming codes are implemented for both production rule retrieval and graphical user interface establishment. The effectiveness of the proposed classifier is illustrated through a real-world application to resolve practical manufacturing problems.

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1. Introduction

1.1. Surface mount assembly

In the electronics assembly industry, printed circuit board (PCB) assembly is an essential part of the manufacturing process, in which surface mount technology (SMT) is an important method used to directly attach the surface mounted components (SMCs) onto the pads of the PCB. SMT assembly consists of three consecutive process steps: solder paste stencil printing, component placement, and solder reflow. In surface mount assembly (SMA), the solder paste is first deposited onto the solder pads of the PCB through stencil printing application, as illustrated in Fig. 1(a) and (b). After this, the pasted boards are mounted with SMCs using a chip placer as depicted in Fig. 1(c). The boards are then conveyed into a reflow oven to form strong electronic connections or solder joints without altering the initial mechanical and electronic characteristics (Lee, 1999), as illustrated in Fig. 1(d). Finally, the assembled boards are visually inspected or tested using an automated optics inspection (AOI) system to identify soldering defects. If soldering failures occur, the defective boards are sent to rework stations for defect correction.

A stainless-steel stencil with designated apertures is used in stencil printing application to transfer solder paste onto a substrate. A squeegee is moved along the stencil surface by air pressure, forcing solder paste through the apertures in the stencil. The stencil is released after the printing iteration, leaving the desired amount of solder paste on the solder pads of the PCB (see Fig. 1(a) and 1(b)). According to industrial reports, 50% to 70% of the total soldering defects are related to the stencil printing process. The printability is influenced by several factors including the stencil design, the constituents of the solder paste, product configuration, and the stencil printer and its printing parameters (Barajas, Egerstedt, Kamen, & Goldstein, 2008; Pan, Tonkay, Storer, Sallade, & Leandri, 2004). Any paste printing faults may result in inferior quality in downstream process steps. For example, incomplete prints may cause a component to be lost during the component placement step or in the formation of insufficient solder joints after solder reflowing. Paste bridges on the other hand may lead to short circuits after soldering. Sometimes a component may not be placed evenly which increases the chances of solder bridge formation between the solder joints.

A chip placer is an automated robotic system dedicated to mounting different types of SMCs onto the PCBs at programmed

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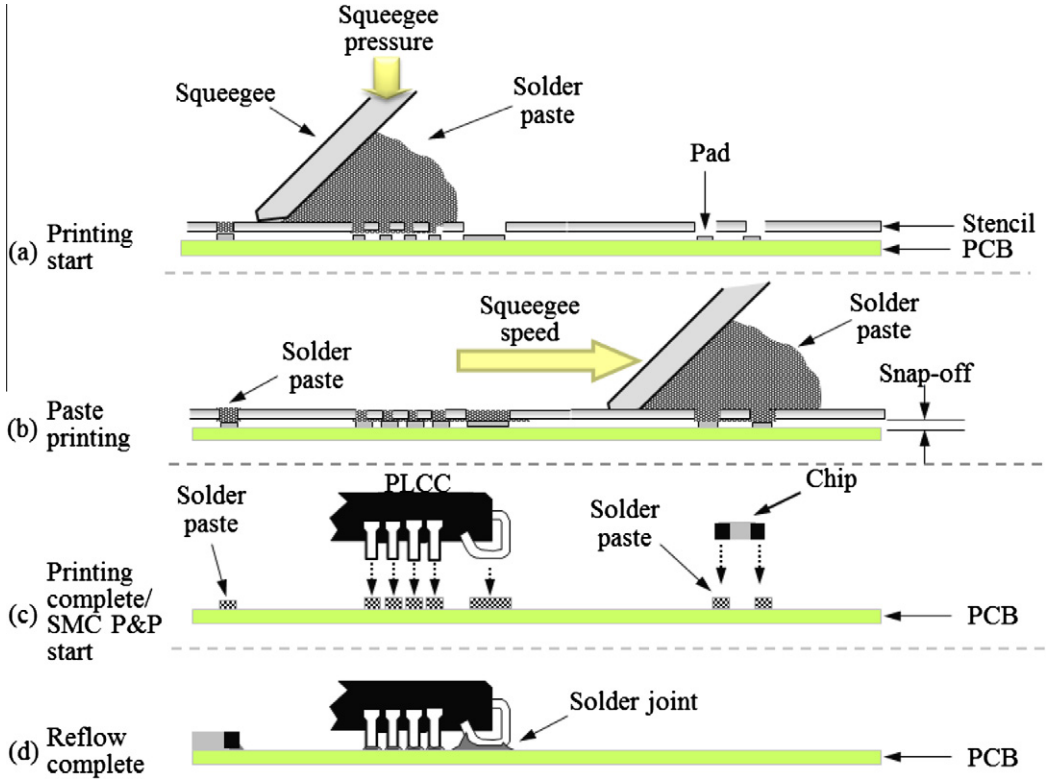

Fig. 1. Surface mount assembly.

locations. A state-of-the-art chip shooter usually provides high placement accuracy, high throughput, and programmable controls. In practice, the precision of placement is identified by the measurements of the *X*-offset and *Y*-offset of the components placed on the boards, as shown in Fig. 2, defined by the distance between the two center points of the component lead and land pads in both the *X* and *Y* directions. Since the scale of significance varies from component to component, the shifting placement is normalized as a fractional number between 0 and 10 (representing the lowest to highest sifting rates) according to IPC standard (IPC-A-610D, 2004).

The solder reflow process is one of the key determinants of product yield (Prasad, 2002). A reflow thermal profile is indicated by a time–temperature graph used to control the heating cycle while the board is reflowed in the oven, as shown in Fig. 3. Both the board and its components are warmed up in the preheating zone, where the board temperature quickly rises from room temperature to about 150 °C. An increase in temperature to 180 °C activates the flux and welts the metallic surfaces of the solder pads and component leads in the soaking zone. In the reflow zone, the solder particles are melted and liquefied. Finally, strong solder joints between component leads and solder pads are formed in the cooling zone. The heating parameter settings such as working mode of the reflow oven, conveyer speed, solder paste ingredients, and number of components assembled can affect the acceptance of a thermal profile. The use of an inadequate thermal profile can generate numerous soldering failures, for example, solder balling, tombstoning, solder voiding, solder bridging, and incomplete solder joints (Lee, 1999; Tsai, 2008).

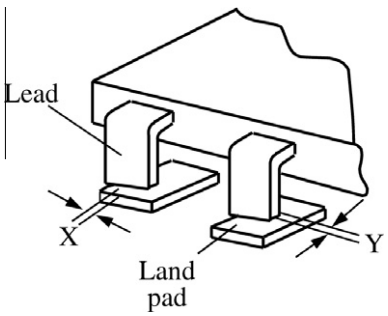

Fig. 2. Precision of component placement.

Defective products lead to an additional 30% to 50% increase in the manufacturing costs due to the additional testing and reworking expenses (Amir, 1994). Therefore, ascertaining the soldering quality is a major issue in the electronics assembly industry. This is particularly evident in the production of telecommunication products due to the reduced size of the devices, extended board complexity, and increased product functionality.

In practice, a soldering failure distribution chart is usually produced to trace the source of soldering defects. A case study is carried out using an anonymous American electronics manufacturer in Taiwan, referred to as company V hereafter, that produces many automated transaction portfolios, including smartcard readers, credit card readers and electronic transaction security systems. This company has a global market share exceeding 50%. The soldering failure distribution chart generated by company V is illustrated in Fig. 4. In summary, stencil printing accounts for 53% of soldering defects, while roughly 17% of the process faults originate from component placement. The other failure sources (30%) are improper reflow soldering and flaws with the raw materials. The map depicts whether failures come from either the stencil printing application, component placement or solder reflow step clearly. However, evidence is absent to identify the source (s) of soldering defects, and how they occur in the steps of the fabrication process is still unknown. Thus, in the real world, engineers improve soldering quality based on experience, by trial-and-error. Yet, the traditional method (i.e., experimental testing) is to examine and optimize a single process step rather than viewing the overall SMA.

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