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Foundry workflow for dynamic-EFA-based yield ramp

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ABSTRACT

The increasing demand for electrical failure analysis (EFA) in yield enhancement [1] has created new challenges for foundries and their clients. Dynamic EFA techniques, more in demand with the smaller technology nodes, have largely been the domain of the design-house failure analysis (FA) lab. In 2010 on 40 nm packaged parts, a new laser-based technology, laser voltage imaging (LVI) was applied to shift debug and drove physical failure analysis (PFA) success rate to >90%. This is still the case in 2011 on 28 nm ICs. The methodology was validated at the foundry on 32 nm wafers and again drove the PFA success rate to >90%. This paper offers a foundry-friendly methodology made possible by LVI and its fast track to the wafer level.

1. Introduction

A surge in the number of defects discovered only at electrical test has created greater demand for dynamic EFA techniques. However, to make these techniques viable in yield operations, they must be foundry-friendly:

1. Dynamic EFA requires a tester. Any alterations to production test patterns would not be a viable solution for the foundry.
2. Dynamic EFA is more efficient when a region of interest can be identified in the GDS chip space. This "map" must be generated at the design house and shipped to the foundry in non-proprietary format.
3. Using Dynamic EFA in the high-throughput environment of the foundry requires less data exchanges and iterations with the design house.

A growing interest in using broken scan chains to drive yield [2,3] was motivation for FA & design for test (DFT) teams to concentrate on an EFA-based shift debug project. The first EFA technique, based on photon emission and good die/bad die comparisons, produced results that were difficult to interpret [4]. The second EFA technique, LVI, effectively isolated the fault to one or two flops plus connected nets, and often times provided additional insight into possible defect types [4,5]. This LVI/shift debug application has been reported to yield >90% PFA success for the die that were analyzed, both at package-level in an FA lab and at wafer-level in a foundry.

2. Laser voltage imaging (LVI) and shift debug

The technology breakthrough came in late 2009 with the rapid adoption of LVI by the FA community. The LVI technology was described in previous works [4].

3. The test pattern

Tester stimulus was very straightforward for this analysis, which is a basic requirement for its adoption at the foundry. We placed the chip in shift test mode and looped on a "11001100..." shift pattern. This created a known frequency in the data stream which was ¼ the shift clock frequency. Two spectrum analyzers, one tuned to the data frequency and one to the clock, could simultaneously capture both data and clock LVI images.

4. Scan flop physical map generation

The initial suspects in a shift debug are the flops in the scan chain. Scan chain "physical maps" were generated in advance using a LEF/DEF-based logical-physical cross-mapping engine [6,7]. Library Exchange Format (LEF) defines the width and height of cells and blocks, including each pin name and location. Design Exchange Format (DEF), an output format generated from place & route tools, defines each cell instance's location and orientation within the chip space. It also defines each net's routing, layer by layer. (However, DEF nets were ignored in this application [8].) DEF format annotates each cell and net with its logical instance name. Therefore, the DEF file(s) for a chip contain both logical and physical information, which can be post-processed into a fast query database. A

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command line query utility does the logical-to-physical translation and generates the map in GDS coordinate space (see Fig. 1).

A common input format for scan chains is Standard Test Interface Language (STIL) This file includes all the flop instance names for each chain, in sequence. The header section of a STIL file specifies which "end" of the chain is the shift output (SCO) and which is shift input (SCI) Other file formats for the scan chains can be substituted, provided they list flops in chain order and include their full hierarchical instance names. The query utility reads the flop list and generates the cell boundaries and pin shapes, replacing each logical instance name with a sequential number. With logical instance names removed, the map is non-proprietary and is therefore approved for foundry use.

Any offsets between DEF and GDS coordinate spaces are adjusted when generating the scan chain physical map. The resulting DEF-derived physical map must overlay accurately in the GDS, since the GDS is used for alignment with the laser scanning microscope (LSM) image and for accurate CAD-to-image overlay [9]. An accuracy of 1-pixel between the LSM and LVI images ensures reliable overlay of cell boundaries on the LVI image.

5. Data exchange between design house and foundry

When a die fails scan chain integrity test, the foundry sends the ATE data log to the design house for isolation of the failing chain. The design house returns failing chain ID and physical map which can be read into the foundry's CAD tool. At this point, LVI analysis can begin (see Fig. 2).

After the stage-to-CAD alignment, the scan chain's physical map is loaded into the CAD tool and sent to the LVI tool as an overlay layer. A binary search technique is used to isolate the failing flop. In recent work on a 28 nm die, an uncompressed scan chain of 30,000+ flops required ten image frames to isolate the failing flop.

6. Data exchange when assisted by chain diagnostics software

When chain diagnostics software [3] can produce a range of flop suspects, the design house can send these flop ID's to the foundry (see Fig. 3). Starting LVI analysis with a small range of flops further increases throughput, since it will require fewer image frames to isolate the failing flop.

The wafer lot characterized in the first LVI shift debug project (done on packaged parts) utilized chain diagnostics software alongside the LVI evaluation. This lot failed shift test on roughly 50% of the die. The diagnostics software classified 33% of these failing die as massive failures (i.e. inconclusive results). It localized 42% of the die to 1–3 chains and another 15% down to 8–10 flops within a single chain. 10% of the die were localized to 1–2 flops. This 10% went straight to PFA.

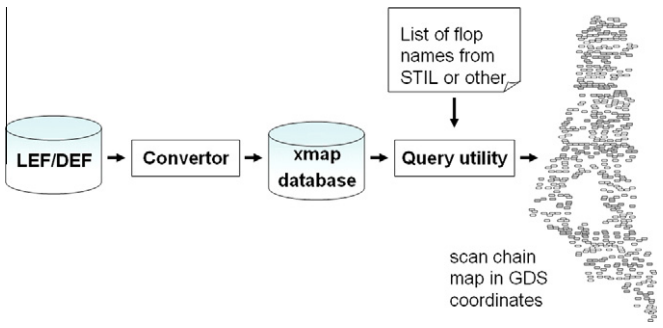

Fig. 1. Conversion of flop instance names to GDS cell boundaries.

7. Wafer-level LVI shift debug at the foundry

LVI analysis at the foundry was done at the wafer level on a 32 nm device. All scan chains were uncompressed and ranged from 6000 to 13,000 flops in length. No chain diagnostics software was used, so this effort represented worst case throughput. Initially, the 50× lens was used as the starting point for the binary search, to identify any dead zone. However, it was soon realized that at 50×, with hundreds of flops in a sea of gates, it was taking too long to adjust the CAD overlay and to interpret the LVI signals within the cell boundaries. For instance, one image frame at 50× was consuming around 8 min to adjust the CAD overlay.

Once the 50× step was removed from the procedure, all wafer-level work was done using either a 350× solid immersion lens (SIL) with 2× zoom or a 175× SIL with 4× zoom. This was effectively a 700× magnification with only tens of flops in a field of view. At this magnification, it was very easy to overlay the CAD and interpret the LVI activity. And ultimately, it required only nine image frames maximum, and six frames on average, to isolate the failing flop.

8. Throughput for wafer-level LVI shift debug

The throughput for LVI shift debug at the wafer level is best explained through time tables. All three tables use the same LVI analysis: a 6000-flop scan chain, and a worst-case binary search efficiency (nine image frames):

Fig. 4 depicts a "cold start" with a new wafer for a new chip. The wafermap must be created in this case. Probe card installation, tester setup and docking were factored in, which took 67 min from setup to flop isolation.

Fig. 5 depicts another wafer for the same chip. The wafermap is already created and tester interface is already established, hence setup time is reduced to just under an hour – 58 min.

Fig. 6 depicts the same wafer, left aligned overnight. By removing the 1 min to unload the wafer, the time table represents die to die stepping. This includes 3 min to land on the die and check continuity, and 42 min of binary search to isolate the flop, for a total of 45 min per die.

9. Defining the PFA area from the first failing flop

To trace the fan-out of the failing flop (C49), the flop was expanded to reveal its pins (Fig. 7, middle). The "Q" output pin was traced using GDS-based physical net trace. (Fig. 7, right, yellow trace.)

Cells attached to the output net were also identified and highlighted from the GDS. The area encompassing the flop fan-out, along with flops immediately before and after the failing flop, were sent to PFA. Hard mask residue on a metal1 to diffusion contact was the defect found by PFA.

10. Summary

LVI shift debug at wafer-level has been proven a viable solution for yield analysis at the foundry. Tester setup is straightforward, scan chain maps are non-proprietary hence design-house-approved, and final defect localization can be performed entirely in GDS. 90% of the die on which we performed LVI analysis yielded good enough results to submit for physical failure analysis. Guided by the LVI results, PFA identified the root cause of the failures in all of the die we submitted. In contrast, guided only by shift diagnosis results, PFA was successful on roughly 10% of the die.