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A simplified yield modeling method for design rule trade-off in interconnection substrates

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Abstract

In this paper, we present a pre-layout yield estimation approach to assess the impact of changing design rules to overall substrate cost. Introducing a density factor for interconnect substrates together with a simplified yield model, thus accelerating the "short failure" critical area estimation, a preliminary design rule trade-off is feasible.

In order to assess a possible cost impact when changing the design rules, we used a nine-chip Pentium multi-chip module as a case study, where we re-calculated substrate sizes and first pass yields using our model. The results showed that there is only a narrow window of opportunity to profit economically from altering the rules. © 2001 Elsevier Science Ltd. All rights reserved.

1. Introduction

High-density substrates are not only required for multi-chip modules (MCMs), present in some of today's leading edge telecommunication and communication products, but also for chip size/scale packages using interposers. The cost for this type of substrates is high, mainly due to the small production panel size operating on outdated 4-in. or 5-in. wafer diameter semi-conductor equipment. In order to improve the cost effectiveness, the European Union Esprit project LAP (Low cost large area panel processing of MCM-D substrates and packages) consortium had the target to setup a large-panel production ranging from 12×12 in.^{2} to 24×24 in.^{2} and to bring down the cost using both production scaling and new materials [1].

While today's 4 in./5 in. thin-film processes are mature and operate under tight control, the new LAP processes are more sensitive to dust particles and other spot defects, exhibiting higher defect density. The reason is that larger clean-room environments are required to process large panels and that the thin-film processes themselves are more difficult to control. Examples for "short/open" defects found on LAP test vehicles so far are shown in Fig. 1(a)–(c). As customers now face lower yield and thus higher cost, the question arises if the use of "relaxed" design rules that are less sensitive to defects can compensate this lower yield.

Given a defect size distribution $s(x)$, the widening of the signal line width and the line–line spacing ("increasing the design rules"), increases the minimum size x_0 of a defect causing a failure. Consequently, the total number of defects that can cause a functional error decreases. An example is depicted in Fig. 2 (adopted from Ref. [2]), where due to expanded line width the fatal defect size $x_{0,A}$ becomes $x_{0,B}$.

On the other hand, the error-susceptible area (the area where the center of a circular-shaped defect the size x has to lie on, commonly referred to as "critical area" CA) grows because there is more interconnection area. Moreover, relaxing the design rules might enlarge the substrate size and therefore its cost. Thus, when relaxing the design rules to be beneficial, the gains due to higher yield have to surpass possible substrate cost increases. Existing work [3] has been confined on the development of local design rules to reduce local fault clusters. But currently, no methodology is available to find the optimum global design rules. With our work we close this

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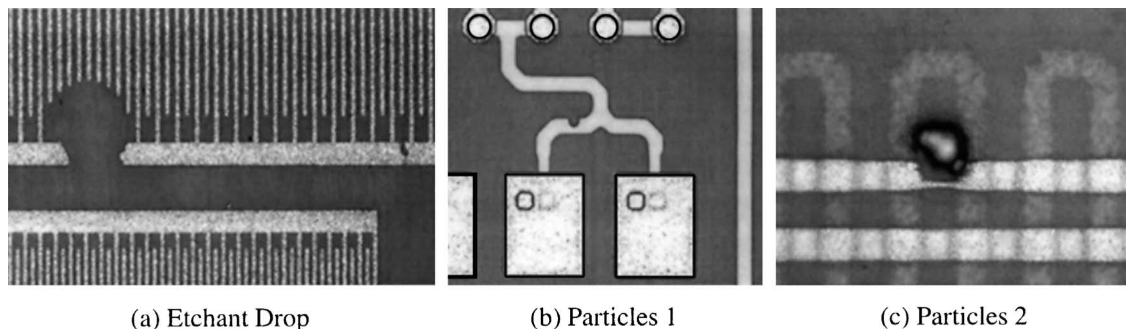

Fig. 1. Typical defects on interconnect substrates, found on process test vehicles.

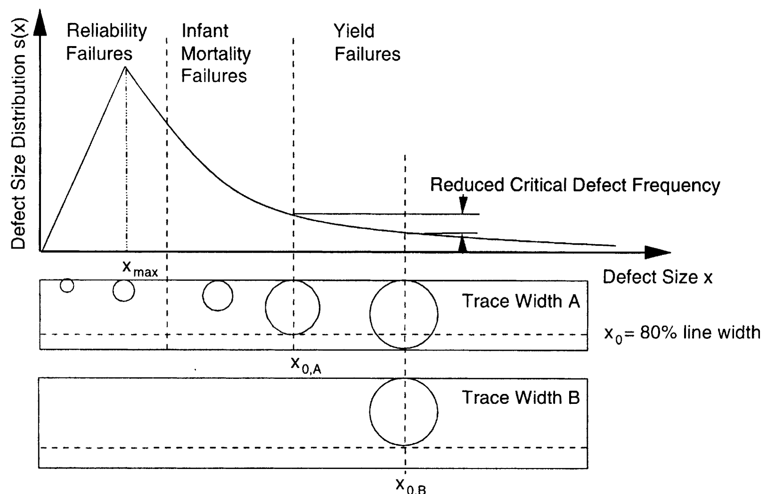

Fig. 2. Defect size probability distribution (adapted from Ref. [2]).

gap allowing for a yield-cost trade-off for high-density interconnect (HDI) substrates.

The paper is organized as follows: first, we briefly review the history and aspects of yield modeling and critical area extraction, then we detail our underlying assumptions and develop the yield vs. line width model. With a case study of a Pentium MCM [4], we quantify the impact on final substrate costs. The results are then discussed, conclusions are drawn, and a brief outlook is given.

2. A yield modeling method for trade-offs

2.1. Existing yield modeling and critical area extraction work

Yield modeling has the goal to predict the yield of a new product or process from existing yield information and various failure models in the yield learning phase of the process. Thus, various approaches exist that aim to predict first pass yield, repair effort, influence of redundant structures or scrap losses based on layout information (see e.g. Refs. [5,6]). The earliest work in this field is reported by Wallmark, Murphy, Seeds, Stapper and others in the mid 1970s for large scale integration (LSI) integrated circuits (ICs).

Among the most known yield models are the Poisson yield model and the negative binomial yield model. Whereas the Poisson model (Eq. (1)) assumes that the spatial distribution of defects is random, the negative binomial model (Eq. (2)) is based on the assumption that the likelihood of a defect occurring at a given location increases linearly with the number of events already occurred, introducing a clustering factor α.

$$\text{Poisson}: \quad Y = e^{-A_C D_0}, \tag{1}$$

$$\text{Negative binomial}: \quad Y = \left(1 + \frac{A_C D_0}{\alpha}\right)^{-\alpha}, \tag{2}$$

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