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Linearly varying surface-implanted n$^-$ layer used for improving trade-off between breakdown voltage and on-resistance of RESURF LDMOS transistor

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Abstract

A new RESURF LDMOS transistor using a linearly varying surface-implanted doped (LVD) n$^-$ layer is reported. Detailed numerical simulations demonstrate the characteristics of this device incorporating an LVD n$^-$ layer and indicate an enhancement on the performance in comparison to an optimal conventional structure with an uniform epi-layer concentration. © 2001 Elsevier Science Ltd. All rights reserved.

Keywords: RESURF LDMOS; Power transistor; Linearly varying surface-implanted doped (LVD) n$^-$ layer

1. Introduction

In recent years, a called reduce surface field (RESURF) lateral device technology for power IC incorporating an uniform n$^-$ epi-layer of the drift region on the substrate silicon wafer has been presented for enabling the lateral breakdown voltage to be increased [1]. This has lead to the rapid development of a low cost high voltage IC process technology.

In early bulk silicon technology, a lateral non-uniform doping profile has been presented to avoid low breakdown voltage caused by the radius of curvature of the metallurgical junction [2]. Continuous graded junction terminations [3,4] are also used for the same purpose. Extending the RESURF principle to SOI technology, Merchant et al. developed a theoretical model for optimizing the breakdown voltage of thin film SOI RESURF LDMOS transistor [5], which predict that the linear lateral doping profile in the drift region on SOI can attain maximum breakdown voltage for SOI RESURF LDMOS [6,7]. A computer program was developed for realization of the linear lateral doping profile and the experimental verifications were also performed [8,9]. However, these results were only available for the thin film SOI RESURF LDMOS devices. As it is well known, the advantages and applications of thin film SOI technology using the RESURF principle are countered somewhat by high cost of the SOI substrate materials and self-heating of the high-voltage power devices.

In this letter, the role of a similar linearly varying surface-implanted doped (LVD) n$^-$ layer implemented at the n$^-$ epi-layer surface of an RESURF LDMOS is investigated using a 2-D device simulation program, MEDICI [10]. The characteristics of this device have been demonstrated compared to an optimal conventional RESURF device and an improvement on the trade-off between the breakdown voltage and on-resistance has been reported.

2. Structure and simulation results

For this investigation, an LDMOS structure with a drift length of 12 μm, substrate doping concentration of 6.5×10^{14} cm^{-3}. and epi-layer thickness of 4 μm is considered. The thickness of the gate oxide and field oxide is 0.04 and 0.6 μm, respectively. The constant concentration of the epi-layer is 1×10^{15} cm^{-3}. The depth of the linearly varying surface-implanted doped n$^-$ layer keep a constant of 0.8 μm. The concentration of the LVD layer varies linearly form a minimum of 1×10^{15} cm^{-3} to a maximum value of 1.5×10^{16} cm^{-3} with a slope of 1.2×10^{19} cm^{-4} as it extends toward the drain region. In the practical devices, the LVD profile can be created using a single phosphorus implant through a mask with a series of openings that are smaller near the source and larger near the drain [4]. For

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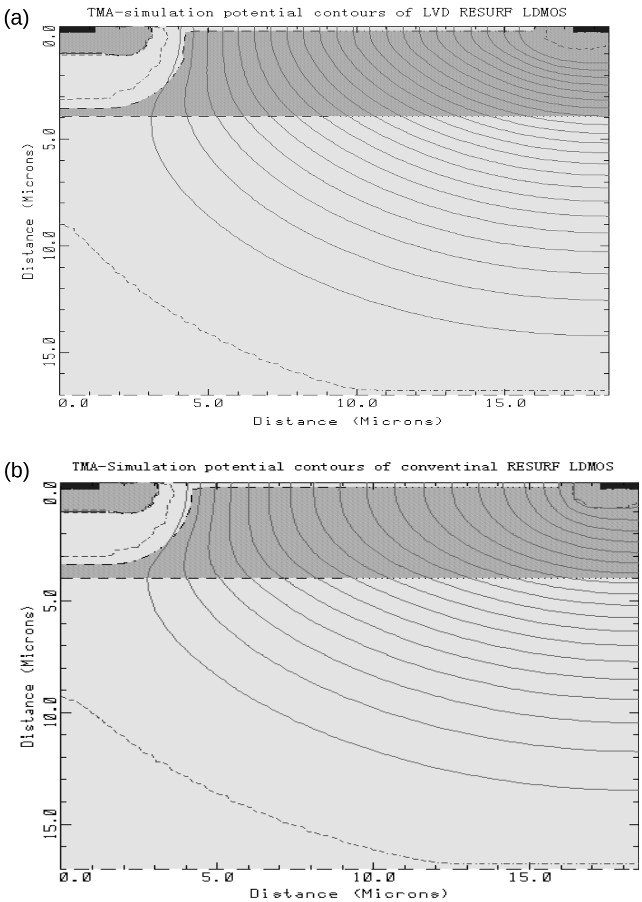

Fig. 1. Simulated potential contours of: (a) proposed LDMOS and (b) conventional RESURF LDMOS with contours = 10 V/step.

the sake of comparison, a conventional but optimal RESURF LDMOS device with the constant drift region doping concentration $2.5 \times 10^{15}\ cm^{-3}$ and epi-layer thickness of 4 μm is simultaneously considered, which has the same drift region length and substrate doping concentration of the LVD device.

Fig. 1 shows the simulated potential contours at breakdown within the proposed LVD and optimal conventional devices. The contours of the LVD device present in an

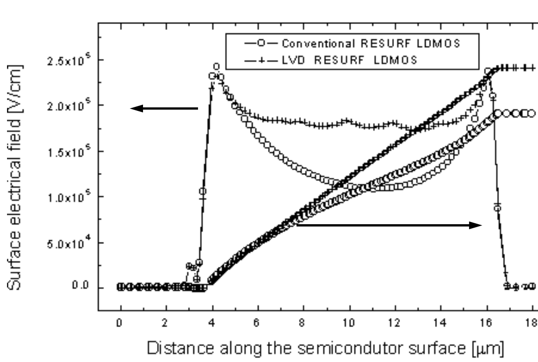

Fig. 2. Surface field and potential distribution of the (O) conventional RESURF LDMOS and (+) LVD-RESURF LDMOS.

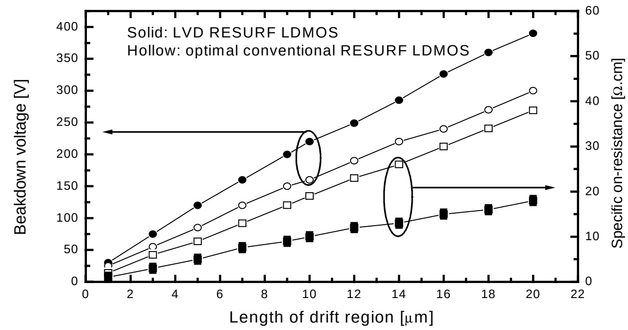

Fig. 3. Trade-off between the breakdown voltage BV and specific on-resistance R_{on} as a function of the drift region length for the (solid) LVD-RESURF LDMOS and (hollow) conventional optimal RESURF LDMOS.

uniform manner thus the avalanche breakdown voltage reaches 245 V while the conventional optimal device shows field crowding at the drain and gate edges and breakdown voltage is limited to 180 V. From here, one can see that the avalanche breakdown of the LVD LDMOS takes place in the bulk region rather than the surface region. In contrast with the novel structure, the breakdown of the conventional LDMOS is determined by an enhanced surface field.

The 1-D surface field and voltage distributions at breakdown are shown in Fig. 2 for both, respectively. As seen in Fig. 2, the field appears non-uniformly for the conventional LDMOS although the two edge peak field near equal. Thus the breakdown voltage is weakened. In contrast, the surface field of the proposed LDMOS is more or less uniform in the entire drift region, leading to an enhancement of the breakdown voltage, an about enhancement factor of 1.5. One can observe the two peak fields at the edge of the drift region, which are intensively related to the effect of the diffusion curvature as shown in Ref. [11] although which has already been reduced compared to the surface field of the conventional structure.

One can find from Fig. 2 that it is just the linearly graded distribution of the voltage that leads to an uniform field profile in the most drift region of the proposed LDMOS. In contrast, the voltage distribution of the conventional RESURF LDMOS shows a large curvature in the whole drift region to lead a non-uniform surface field profile. Consequently, the breakdown voltage suffers a considerable degradation.

We found the LVD LDMOS allowed a significant reduction of the specific on-resistance R_{on} when compared with the conventional RESURF. The numerically calculated values for R_{on} are 23 and 12 Ω cm for the conventional LDMOS and the proposed LDMOS, respectively, yielding an improvement of 50%. In Fig. 3, the variation in the device performance (breakdown voltage/on-resistance) is shown with the different drift region length. Thus, the LVD LDMOS shows a significant advantage over the optimal conventional RESURF.