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Trade off between polysilicon film quality and thin film transistor operational amplifier DC gain

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Abstract

We have fabricated thin film transistor operational amplifiers on a variety of polycrystalline silicon films. We have examined the open loop DC gain of these modules, and have observed that higher quality polycrystalline silicon films usually cause a negative impact on the DC gain of the amplifier. In this paper we have attempted to quantify this relationship, presenting the gain as a function of the transistor mobility, threshold voltage and channel length modulation parameter, which collectively can describe the quality of the active film. We have found that primarily the saturation characteristics of the transistor, as represented by the channel length modulation parameter, and the device threshold voltage have the biggest impact on amplifier gain.

Keywords: Polysilicon; Thin film transistor; Operational amplifier; Gain; Channel length; Modulation parameter

1. Introduction

Thin-film-transistor (TFT) technology presents an exceptionally versatile platform for a variety of applications; some of them are display systems, sensors/actuators and their support electronics, micro-electro-mechanical systems and others. All of these implementations are characterized primarily by their low cost and high level of integration of devices and systems. TFT circuits can be implemented with either amorphous silicon (as the active layer) or polycrystalline silicon MOS transistors. Polycrystalline silicon TFT circuits possess many advantages over those fabricated on amorphous silicon films. This is due to the superior characteristics of the transistors themselves, as indicated by their higher mobility and lower threshold voltage for similar fabrication conditions, and also due to increased design flexibility, which spurs from the ability to fabricate not exclusively n-channel, but p-channel devices as well. Polysilicon TFTs therefore, represent excellent cost effective alternatives to amorphous silicon TFTs in display applications, as pixel transistors and integrated display driver circuits.

Polysilicon films as the active layer for transistors are obtained in a variety of ways, the most common of which are furnace annealing, rapid thermal processing (RTP) or excimer laser annealing of amorphous silicon films. The quality of the resulting polysilicon film is revealed by (among other parameters) the average film grain size and the film trapping density. A number of different experimental measurements for estimating these parameters exist [1]. The quality of the film is also indirectly revealed by the characteristics of the transistors that are fabricated on it; effective carrier mobility and threshold voltage are commonly used to this aim.

Because of the wide field of applications for polysilicon CMOS circuitry, the operational amplifier represents a basic building block of systems that use some form of signal conditioning (amplification, active filtering etc.). This is especially true for sensor/actuator systems that integrate transducer elements with data processing and telecommunication electronics.

We have fabricated simple operational amplifiers as well as other analog and digital circuits for display driver applications, on polysilicon films that have been

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crystallized with a variety of different processes, and their characteristics have been described elsewhere [2]. This work discusses how one of the basic performance measures of the operational amplifier, its DC open loop gain, is affected by the polycrystalline silicon film quality. Indeed, it is of interest that the open loop gain was found to decrease as the quality of the active polycrystalline film improved. It will also be shown that this phenomenon is not confined within the limits of this specific design, but inherent to most amplifier designs.

2. Experimental

For the fabrication of the TFT devices, 100 mm diameter substrates were used. A plasma enhanced chemical vapor deposition (PECVD) SiO_2 barrier layer on the substrate surface was followed by a PECVD deposited layer of amorphous silicon; RTP, excimer laser anneal (ELA) and furnace anneal were employed to crystallize it to polysilicon. A PECVD process was employed to deposit the 100 nm thick SiO_2 film for the gate dielectric. The gate material, amorphous silicon 100 nm thick, was also deposited with PECVD, and after patterning the gate and gate dielectric layers, the drain and source of the device were implanted utilizing ion implantation (phosphorous for n-channel, boron for p-channel devices). This process resulted in CMOS self-aligned devices. Sputtered aluminum was used for the metal layer. All wafers received plasma hydrogenation for 1 h.

A schematic diagram of the fabricated operational amplifier we study is shown in Fig. 1. This is a very common, CMOS, three-stage design without internal compensation. It should be noted though that no stability problems were detected for the given power supply and load conditions. The first stage is a differential pair, comprised of M_1–M_5. Next, a voltage level shifter follows (M_6, M_7), and a class B push–pull amplifier stage are used, to enhance the gain and the output current of the module. Though not a high performance design, this proven amplifier is capable of typical DC open loop gains in the order of 45 dB, with furnace crystallized polysilicon films. A basic limitation of the design is that the saturation current through the input stage (controlled by M_5) and the amount of voltage shifting before the output amplifier are not independently controlled (both are simultaneously set by V_{GG}). A detailed discussion on the amplifier's characteristics can be found in [3].

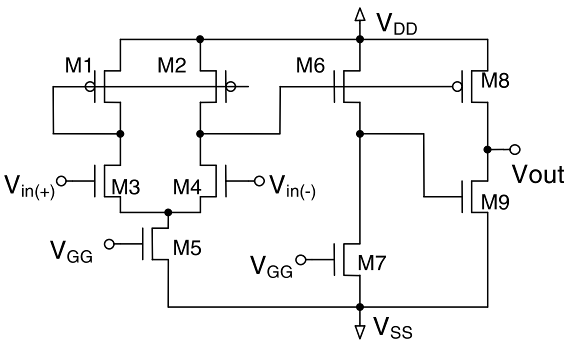

Fig. 1. Schematic diagram of the operational amplifier.

We have simulated this design using the polysilicon TFT models of the AIM-SPICE simulator software. More information on the model parameters may be obtained from [4]. In order to estimate the impact of various parameters that depend on polysilicon film quality on the amplifier open loop gain, we have defined our TFT models to reflect an average device of ours. In this case, it is not important to verify with precision the accuracy of the simulator in absolute numbers, but rather to determine the relative impact of mobility, threshold voltage and channel length modulation parameter on op-amp gain. We have verified our theoretical analysis and simulation conclusions by comparing them to the experimental data.

3. Analysis

The saturation behavior of the TFTs is a crucial factor in the overall performance of the operational amplifier. It is therefore important to understand how it affects the amplifier open loop gain, and how it is affected by the quality of the polysilicon film. Assuming a single-crystal MOS device, we know that in the saturation region, an increase in the drain-to-source voltage V_{DS} results in an increase in the width of the depletion region around the drain, thus decreasing the effective channel length, and increasing the drain current of the device. This phenomenon is represented by the channel length modulation parameter lambda (λ). For single-crystal silicon, lambda may be written as [5]

$$\lambda = \frac{k_{DS}}{L\sqrt{V_{DS} - (V_{GS} - V_T) + \Phi_0}} \qquad (1)$$

where

$$k_{DS} = \sqrt{\frac{2K_S\varepsilon_0}{qN_A}} \qquad (2)$$

where N_A is the channel doping density, Φ_0 is the built-in potential of the channel-drain junction and the rest of the symbols have their usual meaning. For the polysilicon case, N_A may be substituted in (2) by N_{eff}. N_{eff} is an effective channel doping density dependent on polysilicon grain size and trap density, given by [6]

$$N_{eff} = N_{IG} + \frac{2N_{GB}}{L_G} \qquad (3)$$