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Test structure assembly for bump bond yield measurement on high density flip chip technologies

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Abstract

Modern flip chip technologies for imaging applications have achieved a very high integration level together with the possibility of large area assemblies. These developments have resulted in an enormous increase in the total number of bump bonds per assembly. Consequently, yield tests become difficult, and an accurate measurement of it is often discarded. This problem is aggravated in medical applications, where the critical information can be limited to a few pixels, and therefore, yield should be very close to 100%. In these cases, a variation of a small percentage in bump bond yield can make the difference between an usable and a non-usable assembly. Therefore, quantitative and precise measurement of bump bond yield is needed to characterize the quality of any high density flip chip technology for these applications. In this paper, we present a newly developed test structure for electrical measurement of the bump bond yield of high density flip chip technologies, allowing both optimization and statistical control of the process. This test structure facilitates the identification of possible process deviations with precise quantitative yield measurements. It also allows to pin point any localized systematic failure in the bump bonding process. The test structure has been used to evaluate the yield of different flip chip technologies and has contributed to their fine optimization where necessary.

1. Introduction and relevance

Modern detector applications, for X-ray and gamma ray imaging, make use of high density pixel arrays that should be connected with their corresponding readout electronics by means of bump bonding or flip chip technologies. The technology developments achieved lately have increased the density of the pixel arrays by drastically reducing the bump size and the separation between bond pads (pad-pitch). Moreover, the assembly size has increased considerably following a general trend in silicon technologies. These developments have resulted in an enormous increase in the total number of bump bonds per assembly reaching numbers as high as 1 million bump bonds per assembly [1]. As this number increases, quality and yield evaluation of the flip chip technologies becomes difficult, and therefore, an accurate control of the bump bond yield is often discarded to work merely with general estimations of its value.

Test structures and full test chips have been used so far, but only for bond quality tests or for partial yield

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estimations [2,3]. X-ray, infrared or scanning acoustic microscopy (CSAM) are imaging methods that are also applied for yield estimation [4], but they can overpass some electrical problems and they are impractical for quantitative measurements in large assemblies.

The problem is aggravated in applications involving medical imaging, since the critical information can be limited to a few pixels, and therefore, yields should be very close to the 100%. In these cases, a variation of a small percentage in bump bond yield can make the difference between a usable and a non-usable assembly. Moreover, the recent introduction of new techniques and materials in the bump bonding processes [5] makes previous yield figures in the hands of the manufacturers not valid anymore for these new technologies and emphasize the need of properly updated yield measurements.

For these reasons, precise and quantitative measurements of bump bond yield are needed to characterize the quality of modern flip chip technologies, but, at the moment, there is not a valid tool in the hands of the manufacturers to obtain accurate yield figures of their flip chip technologies. In the same way, there is not a valid method for the end users, like image application developers, to compare among different manufacturers in terms of yield figures. The only possibility is to directly use their "precious" real detectors and chips in test prototypes and estimate the bump bond yield with the resulting images from those prototypes. This has the inconvenient that there is no way to know whether a bad image pixel comes from bump bonding problems or problems in the original detector or chip, or even in the readout system.

In this paper, we present a newly developed test structure that allows quantitative electrical characterization of the bump bond yield of a technology, allowing statistical control of the process. The test structure consists of a full assembly with a practical number of long bump bond daisy chains evenly distributed across the whole assembly. By measuring the conductivity of these chains through the whole assembly, the bump bond yield can be obtained with a statistical calculation. The number of bump bonds per chain can be tuned in order to adjust the test to the yield ranges of interest for the particular application. This test structure has been used on different flip chip technologies in order to measure their yield and perform quantitative comparisons.

2. Test structure description

The new test structure that has been designed consists of an array of bump bonds, in which a certain fraction of them (approximately one third of them) have been connected, in one direction, by metal lines to form daisy chains, and the rest are short-circuited, in the same direction, to connect the daisy chains to the external pads. The test structure is therefore, a full assembly made of a series of long bump bond daisy chains that are evenly distributed across the whole area of the assembly. Each daisy chain contains L bump bonds, connected in a way that if any of them fails, the whole chain is electrically open. Fig. 1 shows a schematic cross-section of a daisy chain in the assembly. The chains are then connected to test pads prepared for automatic measurements with an automatic probe machine. The test structure is actually a whole assembly, and therefore, composed of two sides for the flip chip process. One of them is the "chip" side (c-side) with the metal pattern to make one half of the daisy chains, plus the corresponding fan-out to the test pads for automatic testing. The "detector" side (d-side) contains only the corresponding metal pattern to match with the c-side forming the daisy chain structure. The daisy chains are uniformly distributed in the test structure in order to cover the whole assembly area. In addition, two ground busses, with all their bump bonds short-circuited, cross the assembly in perpendicular directions roughly at the middle of the assembly in order to facilitate the connection of the daisy chains to ground for the testing.

In the particular case of the test structure assemblies used in this work for the technology comparison described below, the assemblies are arrays of 256×256 bump bonds with 55 μm pitch. Each daisy chain has 50 bump bonds and each assembly has 504 independent daisy chains. In this way, two fifths of the total bump bonds of the assembly are connected to a daisy chain, and contribute to the statistics, while the rest are short-circuited in one direction (the same of the daisy chains). The daisy chains are then connected to the test pad arrays using a 1×16 probe card configuration. A detail of the central ground bus area of the fabricated d-side of the test structure assembly can be seen in Fig. 2, while Fig. 3 shows a picture of an example of the actual test structure assemblies tested for this work. In this figure, the test pad arrays with their fan-out from the daisy chains can be seen at both edges of the c-side part of the assembly, while, on top of it and upside down, the d-side of the assembly can be seen.

Electrical resistivity measurements are performed between each of the test pads connected to each of the daisy chains in the test assembly, and the pads connected to the ground bus. If the resistance value obtained for a

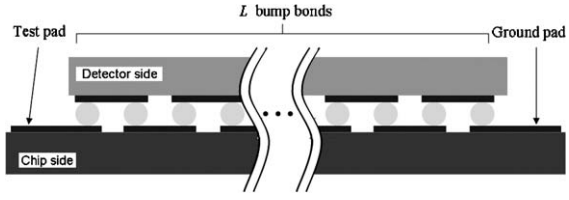

Fig. 1. Scheme of the daisy chain concept.