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Strain sensitivity of gate leakage in strained-SOI *n*MOSFETs: A benefit for the performance trade-off and a novel way to extract the strain-induced band offset

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The impact of biaxial stress on gate leakage is investigated on fully-depleted silicon-on-insulator (FD-SOI) *n*MOS transistors, integrating either a standard gate stack or an advanced high-κ/metal gate stack. It is demonstrated that strained devices exhibit significantly reduced leakage currents (up to −90% at E_{ox} = 11 MV/cm for $\sigma_{tensile}$ = 2.5 GPa). This specific effect is used to extract the conduction band offset ΔEc induced by strain and is shown to be accurate enough to monitor stress in MOSFETs. This new technique is much less sensitive to gate oxide defects than the method based on the threshold voltage shift ΔV_T. This accurate experimental extraction allowed us to pick out realistic values for the deformation potentials in silicon (Ξ_u = 8.5 eV and Ξ_d = −5.2 eV), among the published values.

1. Introduction

Strained silicon films have been recently introduced in CMOS technologies to boost mobility performance of metal–oxide–semiconductor field-effect-transistors [1–3]. The modification of the silicon band structure induced by biaxial strain also affects the threshold voltage Vt [4,5] and the gate leakage current density Jg [6–10], which has strong implication on circuit performance by reducing power consumption. Although accurate knowledge of the deformation potential values would be useful for modelling tools, there is still no consensus about their exact values, as shown by the various set of parameters found in the literature [11–13] (see inset of Fig. 3). In this paper, we propose to use the strain sensitivity of gate leakage to give realistic parameters. Results are compared to those obtained from an extraction based on the Vt shift, ΔV_T.

2. Experimental details

Lightly p-doped undoped (Na = 10^{15} at/cm^3) SOI and strained-SOI (sSOI) substrates have been used for this analysis [14]. The sSOI substrates have been fabricated using a relaxed $Si_{1-x}Ge_x$ starting buffer layer with Ge content of 20%, 30% and 40%. The top Si layers have then been thinned down to 10 nm by sacrificial oxidations. Thanks to this process, sSOI substrates do not suffer from Ge out diffusion towards the gate oxide interface [15,16] since the starting SiGe layer is removed before device processing (Inset of Fig. 1).

The tensile biaxial stress σ induced in the Si films was measured by Raman spectroscopy. It was estimated to 1.3 GPa, 2.0 GPa and 2.5 GPa, corresponding to an in-plane deformation $\varepsilon_{//}$ of 0.72%, 1.1% and 1.38%, respectively (Fig. 1). The amount of stress in the SOI film was proportional to the Ge content *x*, apart from a small relaxation for *x* = 40%.

*n*MOSFETs have then been fabricated using a conventional process flow. A 5 nm SiO_2 film (t_{ox}) was thermally grown and a *n* + (10^{20} cm^{-3}) highly-doped poly-silicon film was used as gate electrode. As a consequence, the threshold voltage Vt was negative, as shown in Fig. 2 (Vt = −0.12V for unstrained-SOI devices). The resulting EOT is around 4.8 nm, as determined by fitting *C–V* measurements to 1D Poisson–Schrödinger simulations. Measurements have been performed on 10 × 10 μm^2 devices.

3. Results and discussions

3.1. Mobility

A 75% and 90% electron mobility (μ_e) gain at high electrical field (at N_{inv} = 10^{13} cm^{-2} corresponding to Eeff ~0.78 MV/cm) was obtained for sSOI 20% and 30%, respectively (Fig. 1). Such an increase

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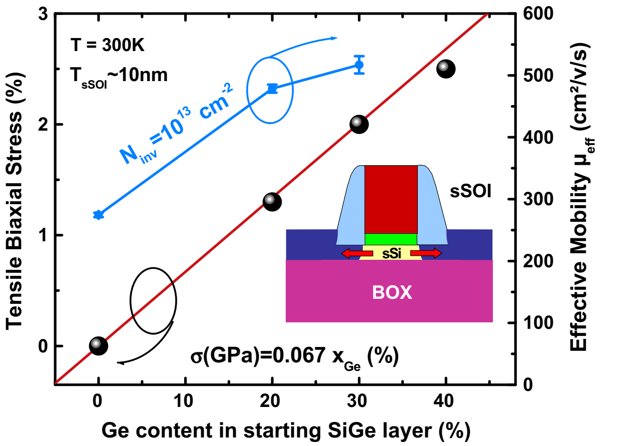

Fig. 1. Tensile biaxial stress (left axis), measured by μ-Raman, and electron effective mobility (right axis) in strong inversion ($N_{inv} = 10^{13}$ cm^{-2}), extracted by the split *C–V* technique (dispersion on 40 dies), versus the Ge content in starting $Si_{1-x}Ge_x$ relaxed substrate. Inset: schema of a sSOI device. Note that Ge sources have been removed before device processing.

has been repeatedly observed [1,2] and attests that the initial strain is maintained in the final processed device.

3.2. Threshold voltage

Figs. 2 and 3 show that Vt decreases linearly with σ. Assuming an ideal gate oxide (no interface states and no fixed charges), the threshold voltage in FD-SOI single gate devices can be analytically expressed as [17]:

$$\mathrm{Vt} = \phi_M - \chi_{Si} - \frac{\mathrm{Eg}_{Si}}{2} + \frac{k_B T}{q}\ln\left(\frac{C_{ox} k_B T}{q^2 t_{Si} ni_{Si}}\right) + \frac{h^2\pi^2}{8qm^{*,c}_{Si} t^2_{Si}} \quad (1)$$

It depends on the temperature T, the properties of the Si film (i.e., the electron affinity χ_{Si}, the silicon bandgap Eg_{Si}, the film thickness t_{Si} and the intrinsic carrier concentration ni_{Si}) and on the gate and oxide parameters (i.e., the gate workfunction ϕ_M and the oxide capacitance C_{ox}). The last term takes into account the variation of Vt due to carrier confinement at the top interface. It depends on the effective electron mass $m^{*,c}_{Si}$ in the confinement direction [0 0 1] and on t_{Si} · k_B and h are Boltzmann's and Planck's constants, respectively. q is the electronic charge. Given that $ni_{Si} = \sqrt{\mathrm{Nc}_{Si}\mathrm{Nv}_{Si}}\exp(-\mathrm{Eg}_{Si}/2)$, the Vt shift $\Delta\mathrm{Vt} = \mathrm{Vt}^{sSOI} - \mathrm{Vt}^{SOI}$ induced by the biaxial strain is thus given by:

$$\Delta\mathrm{Vt} = -(\chi_{sSi} - \chi_{Si}) - \frac{k_B T}{2q}\ln\left(\frac{\mathrm{Nc}_{sSi}\mathrm{Nv}_{sSi}}{\mathrm{Nc}_{Si}\mathrm{Nv}_{Si}}\right) + \frac{h^2\pi^2}{8qt^2_{Si}}\left(\frac{1}{m^{*,c}_{sSi}} - \frac{1}{m^{*,c}_{Si}}\right) \quad (2)$$

As the effective carrier masses hardly changes with biaxial strain [18–20], the second and third terms can be neglected (~8 mV and ~0.3 mV, respectively, at worst for $x_{Ge} = 0.4$, i.e., less than 5% of the experimental ΔVt). Therefore, in FDSOI devices, ΔVt can be directly linked to the conduction band offset ΔEc = -($\chi_{sSi} - \chi_{Si}$). Using the $\langle 1\,0\,0\rangle$ strain tensor [11], it is expressed as

$$\Delta\mathrm{Vt} = \Delta\mathrm{Ec} \approx \Delta\mathrm{Ec}^{\Delta 2} = \Xi_d(2\varepsilon_{//} + \varepsilon_\perp) + \Xi_u\varepsilon_\perp \quad (3)$$

where $\varepsilon_{//}$ and $\varepsilon_\perp$ are the in-plane and the normal components of the strain tensor, respectively. Ξ_d and Ξ_u are the dilatation and uniaxial deformation potential coefficients of the Herring's theory [21], respectively.

The experimental ΔVt values have been compared to this model in Fig. 3. The best fit was obtained with the values Ξ_u and Ξ_d proposed by Kanda [13] and given in the inset of Fig. 3.

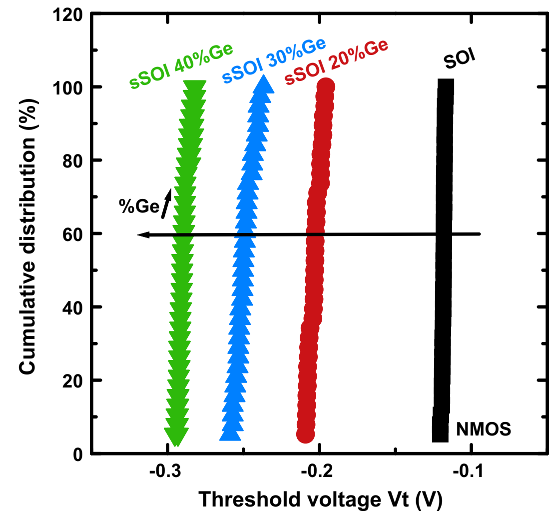

Fig. 2. Cumulative distributions of threshold voltages Vt obtained on 40 SOI and sSOI *n*MOSFETs at room temperature. Vt is very well controlled and is shifted negatively with increasing strain in the Si film.

3.3. Gate leakage

The gate leakage current densities Jg in unstrained and strained devices were compared in Fig. 4 as a function of the oxide field E_{ox}. In the trap-assisted-tunneling regime (TAT) [22,23], Jg weakly depends on strain since it is rather controlled by the trap density in the oxide. In contrast, in the Fowler–Nordheim regime (Fig. 6, $\phi_b < q \cdot V_{ox}$), Jg^{sSOI} was reduced at same E_{ox} compared to Jg^{SOI}. This reduction is plotted in Fig. 5 versus stress level.

Considering that there is only one injection level, the lowest energy level $E_0^{\Delta 2}$ [24,25], and that the effective barrier $\phi_b - E_0^{\Delta 2}$ is almost constant in the FN regime, as proposed by Weinberg who considered a constant mean value for $E_0^{\Delta 2}$ [24,25], a simple method, based on the FN classical expression, is then proposed to extract the barrier height ϕ_b (Fig. 6):

$$J_{FN} = A \cdot E^2_{ox} \cdot \exp\left(-\frac{B^*(\phi_b^{FN})^{3/2}}{E_{ox}}\right) \quad (4)$$

$$\text{with} \quad A = \frac{q^3(m^{*,c}_{Si}/m^{*,c}_{ox})}{8\pi h\phi_b^{FN}} \quad (5)$$

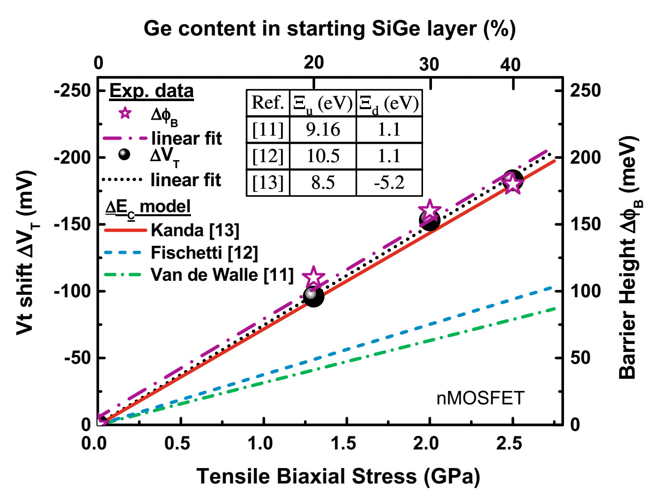

Fig. 3. Strain-induced variations of Vt ($\Delta\mathrm{Vt} = \mathrm{Vt}\sigma - \mathrm{Vt}^0$) and of barrier height ϕ_b ($\Delta\phi_b = \phi_b^\sigma - \phi_b^0$) with respect to the stress in the (0 0 1) plane. Inset: potential deformation values found in the literature. Experimental data are in very good agreement with Kanda's values.