Microelectronics Reliability 52 (2012) 525–529

Contents lists available at SciVerse ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Trades-off between lithography line edge roughness and error-correcting codes requirements for NAND Flash memories

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ARTICLE INFO

Article history:
Received 17 June 2011
Received in revised form 2 September 2011
Accepted 19 September 2011
Available online 24 January 2012

ABSTRACT

The only way to keep pace with Moore's Law is to use probabilistic computing for memory design. Probabilistic computing is 'unavoidable', especially when scaled memory dimensions go down to the levels where variability takes over. In order to print features below 20 nm, novel lithographies such as Extreme Ultra Violet (EUV) are required. However, transistor structures and memory arrays are strongly affected by pattern roughness caused by the randomness of such lithography, leading to variability induced data errors in the memory read-out. This paper demonstrates a probabilistic–holistic look at how to handle bit errors of NAND Flash memory and trades-off between lithography processes and error-correcting codes to ensure the data integrity.

1. Introduction

The NAND Flash memory is a widespread storage media, due to its fast Non-Volatile (NV) high capacity storage. This type of memory based Solid State Drives (SSDs) is the main replacement candidate for conventional Hard Disk Drives (HDDs). The evolution of NAND Flash is supported by two main trends: memory cells are pushed into smaller geometries, and Flash cell architectures are moving to store more bits per cell [1]. However, there are obstacles against NAND Flash scaling. Vertical Floating Gate (FG) transistor scaling is limited by insulators shrinking. Furthermore, the lateral dimension scaling leads to a cell-to-cell (or cross-cell) interference [2,3]. The cell-to-cell interference, which is caused by parasitic capacitive coupling between neighboring FGs, is recognized as a major hurdle for memory cell scaling [4]. Moreover, the effect of parasitic interference is data dependent in highly scaled NV memories [5], thus requires complex statistical simulation for modeling.

Advanced lithography such as EUV and Double Patterning (DP) processes are required to reach Flash densities doubling every year. Line edge roughness (LER) is one of the main effects of process uncertainties in EUV lithography. All of the lithographic elements, such as source, mask, optical system and resist, and contribute to LER [6]. LER is the outcome of the stochastic behavior of photons, photogenerated electrons, polymer resist erosion and acid-based annihilation. By itself, LER induces random deformations in size and spacing of the transistors [7,8]. Moreover, it forms structural bending of a memory array [9,10]. The cross-cell interference between the memory cells is strongly affected by gate spacing variations of the array. The pattern roughness of FG transistor structures is significant compared to the transistor sizes and sufficient to cause variations of the parasitic cross-cell interference and to degrade the memory functionality [11]. These variations lead to stronger overlap and broadening of programmed threshold voltage V_{th} windows than would be expected in a memory array without LER. The overlap of V_{th} windows, due to the variable cross-cell interference, leads to error generation in a memory readout [12].

Various post-lithographic techniques exist for LER mitigation: in-track chemical processes, ion beam sputtering, thermal and plasma treatments [13,14]. The smoothing processes are able to reduce LER up to 35%, at the expense of an increased manufacturing cost. To keep the error rates (caused by variability) under a certain acceptable threshold, advanced error correcting codes (ECC) are used. The more variability triggers data errors, the stronger and more complex error control techniques are required. The complexity of the on-chip or on memory controller running ECC brings extra requirements for memories such as: chip area and power dissipation, as well as impact on access time [15,16].

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0026-2714/$ - see front matter © 2012 Elsevier Ltd. All rights reserved.
doi:10.1016/j.microrel.2011.09.037

In this case study, 16 nm half-pitch (hp) NAND Flash memory was treated as communication channel. As the fault tolerance technique, Bose–Chaudhuri–Hochquenghem (BCH) and Low Density Parity Check (LDPC) codes were applied on the channel model including LER induced variability.

In this paper, based on our previous research work, a holistic framework is proposed to trade-off the lithographic processes and the ECCs in highly scaled NAND Flash memories. The presented framework statistically percolates the variations caused by LER of advanced lithographies and post-lithography techniques all the way up from the material level to the system level. The presented probabilistic tool helps to evaluate the reliability improvement via LER smoothing processes or by boosting the error correcting complexity by adding more parity bits and/or usage of more advanced codes. The rest of the paper is organized as follows: Section 2 describes LER modeling techniques, in Sections 3 and 4 simulation results are shown followed by the conclusions.

2. LER of lithography and post-lithography processes

Fig. 1 presents 32 nm hp printed lines in 193 nm immersion double pattering lithography and EUV lithography before and after LER smoothing post-lithography technique. Lithographic patterns were realized by ASML imec Alpha Demo Tool (ADT). ADT uses discharge produced plasma to generate EUV photons at 13.5 nm wavelength. In this case study, EUV wafers were realized by exposing a 4× binary mask using a conventional illumination with $\sigma_{out} = 0.5$ and NA = 0.25. State of the art EUV resist on 24 nm underlayer was used. The LER reduction was obtained with high-energy argon sputtering process. The main idea is to use an implanter tool at grazing incidence, parallel to the printed lines, in order to reduce the protrusion at the edges of the lines [13,14].

Characterization of LER is performed in the following way: Scanning Electron Microscope (SEM) images were captured; then image processing is performed to detect the edges of the printed lines (zero-cross method): Critical Dimensions (CD) and Power Spectral Density (PSD) are therefore obtained. Since LER is feature-dependable effect, it is extracted upon pattern sizes from the PSD (Fig. 2). Also LER is a natural limitation of any lithography process; moreover LER remains as the device shrinks and becomes more important for tiny devices. This issue leads to serious device fluctuations and performance degradations.

All material level discrepancies bring more randomness into memory functionality, finally decreasing reliability. Hence, smoothing post-lithography techniques are likely to be considered in a device process flow in order to meet the ITRS (International Roadmap for Semiconductors) targets for the future technological nodes. For EUV lithography it will be particularly true, due to its higher roughness outcome, compared to current lithography technique (193 nm immersion, multiple patterning approaches, and direct self assembly). Each of the elements used in a EUV lithography process increases the uncertainty of the process, worsening the final LER [17,18]:

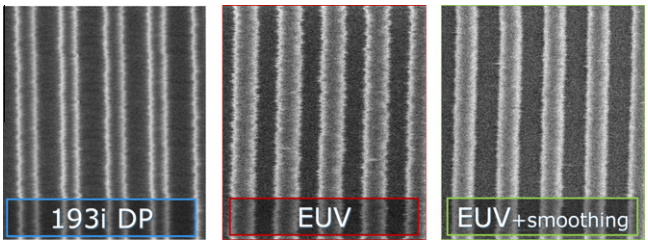

Fig. 1. SEM-CD top-down images of LER affected printed lines.

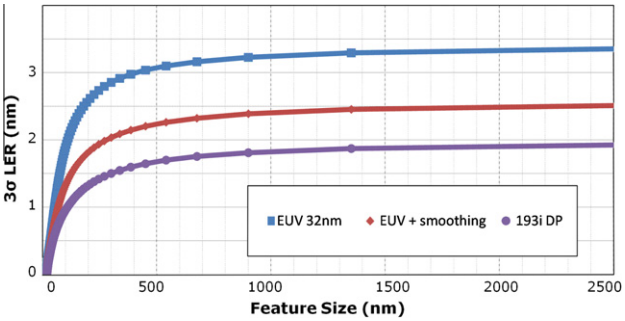

Fig. 2. LER variations upon the feature sizes.

- EUV source with the speckle effect (source intensity fluctuation) and the photon shot noise.
- Mask non-idealities due to its fabrication process, as surface and absorber roughness.
- Optical system non-flatness and flare effect.
- Resist stochastic response to high-energy photons absorption: secondary electron blur, acid shot noise, base-acid annihilation, polymer deprotection and development threshold fluctuation.

The more lithography will approach to its natural limit, the worse LER will become, due to a discrete behavior of the nature which cannot be neglected at these feature sizes.

3. Variability percolation modeling

Accurate results can be obtained by modeling all possible error generating factors from a material level to a system level of a memory. Fig. 3 shows the flow of variability percolation from the material level up to the system level. At the material level, LER caused transistor structures variations and spacing distortions of an array are translated into the variations of parasitic capacitive couplings, and consecutively, affect variations of V_{th} of each cell. The variability of

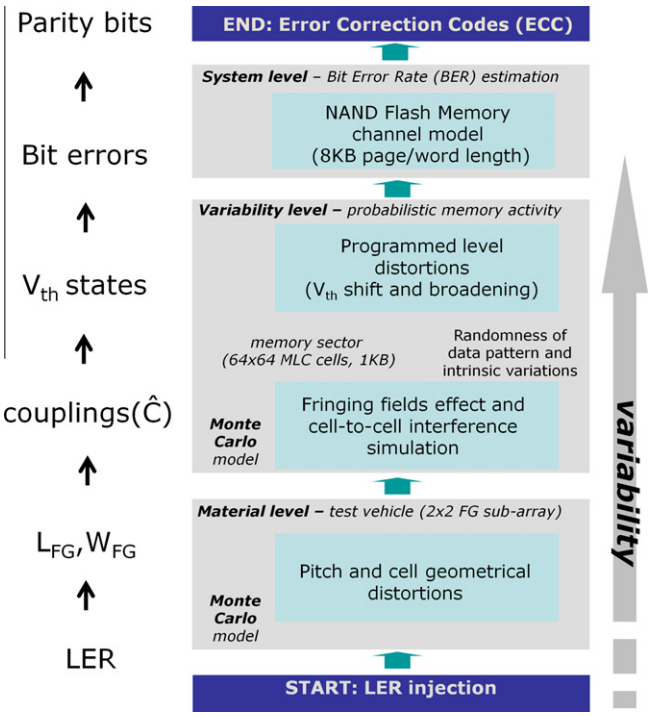

Fig. 3. Variability percolation – flow chart.