Available online at www.sciencedirect.com

ScienceDirect

Microelectronic Engineering 84 (2007) 2817–2831

MICROELECTRONIC ENGINEERING

www.elsevier.com/locate/mee

Chemical mechanical planarization operation via dynamic programming

Chia-Shui Lin [a,*], Yung-Chou Lee [b]

[a] *Department of Mechanical Engineering, National Chiao Tung University, Hsin-Chu 30050, Taiwan*
[b] *Department of Electrical and Control Engineering, National Chiao Tung University, Hsin-Chu 30050, Taiwan*

Received 28 April 2006; received in revised form 1 December 2006; accepted 5 February 2007
Available online 16 February 2007

Abstract

In this paper, the impact on non-planarization index by the down force and rotational speed during a SiO_2 or Cu CMP process was investigated. Since the magnitudes of down force and rotational speed have limits, we choose the dynamic programming approach because of its ability to achieve constrained optimization by the down force and rotational speed. The duration and the amount of input were computed based on the chemical mechanical polishing model by Luo and Dornfeld [J. Luo, D.A. Dornfeld, IEEE Trans. Semiconduct. Manufact. 14(2) (2001) 112–132.] when the other parameters were fixed. Experiments done for blanket wafers based on dynamic programming operation and conventional constant removal rate operation was compared with each other. The non-planarization index could be improved consistently by dynamic programming operation versus constant removal rate operation. The improvement ranges from 2% to 39% improvement over the base recipe of constant removal rate in all experiments as shown in Tables 3 and 6. The thickness removal error is consistently smaller by constant removal rate operation versus dynamic programming operation in all experiments as shown in Tables 3 and 6. To get the best performance of both planarization and thickness removal, it is recommended that planarization step and overpolish step in SiO_2 and Cu CMP should use different mode of operation, i.e., dynamic programming operation during planarization step for minimizing non-planarization index and constant removal rate operation during overpolish step for minimizing thickness removal error. The incremental time calculation for eliminating thickness removal error during overpolish step can be done using the thickness error and removal rate derived from Luos' removal rate model based on constant wafer pressure and platen speed at the end of planarization step.

Our contribution is a new approach for CMP. Standard CMP uses constant removal rate operation in both planarization step and overpolish step. Our new approach uses dynamic programming operation during planarization step and constant removal rate operation during overpolish step.

Keywords: Chemical mechanical planarization; Dynamic programming; Non-planarization index; Copper dishing; Oxide erosion

1. Introduction

Chemical mechanical planarization (CMP) is a widely accepted technique to provide a globally planarized surface for microelectronic wafer fabrication nowadays. CMP was developed during the early 1980s when multilevel interconnect technology was pushed to the limits of circuit density and performance. This technique produces excellent planarization across the wafer surface and improves both photolithography and deposition process [1]. In recent years, the device levels and densities increased continuously, at the same time the problem of resistance–capacitance (RC) time delays which can appreciably slow down circuit speeds must be solved quickly. As a result, copper has emerged as the optimal interconnect material because of its low resistivity and high electromigration resistance compared with aluminum [2,3]. Patterned Cu lines are produced by a damascene process when using Cu as an interconnect material. In the damascene process, the dielectric is patterned, followed by the barrier and metal deposition. The barrier is required to prevent the rapid diffusion of the

* Corresponding author. Tel.: +886 35731796; fax: +886 35720634.
E-mail address: chiaslin@mail.nctu.edu.tw (C.-S. Lin).

0167-9317/$ - see front matter
doi:10.1016/j.mee.2007.02.003

Cu into the dielectric. The final step in this process is CMP that removes the excess metal and provides global planarization. Fig. 1 schematically shows a single layer Cu interconnect structure before and after CMP. Two key problems in Cu pattern wafer CMP, namely copper dishing and oxide erosion, generate surface non-planarity which gives rise to problems in integrating multiple layers of metal. Copper and oxide thinning results in increased RC delay which leads to inferior device performance. Therefore, we focus on the experiments for SiO_2 and Cu CMP.

Several research efforts have been reported on modeling the CMP process and the most well known equation is the Preston's equation [4]. Preston's equation reflects the influence of process parameters including wafer pressure and relative velocity. In the last several years, the revised Preston's equations concentrated on different elements of CMP. For example, Zhang and Busnaina [5] proposed an equation taking into account the normal stress and shear stress acting on the contact area between abrasive particles and wafer surfaces. Tseng and Wang [6] showed that the removal rate is proportional to the terms $P^{5/6}$ and $V^{1/2}$. Zhao and Shi [7,8] consider the effects of the pad hardness and the contact between wafer and pad. Luo and Dornfeld [9] assumed an indentation-sliding model for the penetration of the pad and included an empirical accommodation of chemical reaction at the wafer surface. Compared with experiment results, the Luo and Dornfeld model more accurately predicts the removal rate. (Therefore, the Luo and Dornfeld model will be employed to predict thickness removal rate in this paper).

Most of the research work on CMP is focused on removal mechanism and slurry chemistry. Chiu et al. [10] applied the concept of soft landing of a spacecraft to CMP operation. Therefore, the CMP operation can be formulated as a minimum time optimal control problem. They treat the oxide surface as the landing surface, the polishing pad as a fly vehicle, and the removal rate as the vertical velocity. The equations describing the thickness removal process can be expressed as:

$$\begin{bmatrix} \dot{H} \\ \dot{R}R \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} H \\ \mathrm{RR} \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} a$$

$$-a_{\max} \leqslant a \leqslant a_{\max}$$

where H is the thickness of material to be removed, RR the removal rate, and a the rate of change of the removal rate. The constraints in removal rate and rate of change of removal rate are applied because the parameters of CMP machine have physical limit, e.g., platen speed, wafer pressure, and slurry flow rate. They also set the final condition to $H(t_f) = 2000$ Å and $RR(t_f) = 2000$ Å/min in order to reduce the dishing and erosion according to the experimental data proposed by K. Wijekoon and S. Tsai etc. [17]. Fig. 2 shows that copper dishing and oxide erosion are proportional to platen speed and wafer pressure. Once the landing point is reached ($H(t_f) = 2000$ Å), the polisher continues the removal with the smaller removal ($RR(t_f) = 2000$ Å/min) until the end point is detected. Fig. 3 shows the result of optimal operation. Through their inspiration, we plan to use dynamic programming as our method of optimal operation in this research.

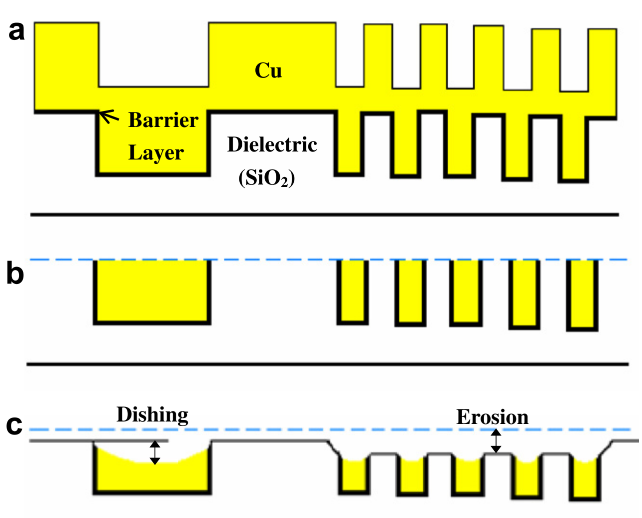

Fig. 1. Schematics of a single layer Cu interconnect: (a) before polishing, (b) ideal case after polishing and (c) real case after polishing.

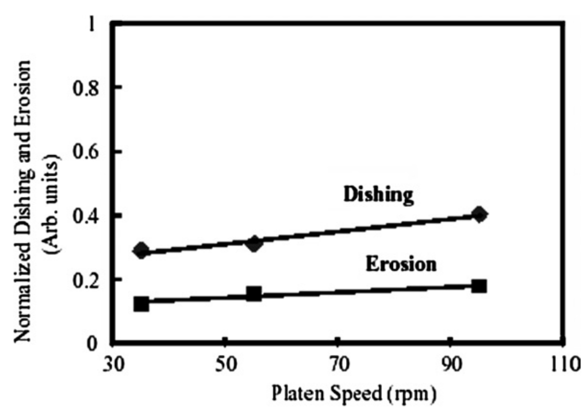

Fig. 2a. Dependence of copper dishing and oxide erosion on platen speed. Wafer pressure was kept constant [17].

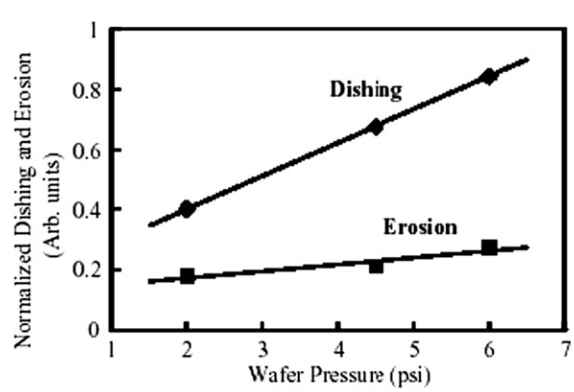

Fig. 2b. Dependence of copper dishing and oxide erosion on wafer pressure. Platen speed was held constant [17].