Microelectronics Reliability 52 (2012) 1559–1564

Contents lists available at SciVerse ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Reliability optimization of analog integrated circuits considering the trade-off between lifetime and area

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ARTICLE INFO

Article history:
Received 12 August 2011
Received in revised form 28 September 2011
Accepted 30 September 2011
Available online 21 October 2011

ABSTRACT

The reliability of analog integrated circuits becomes a major concern for the semiconductor industry as technology continuously scales. Among the many contributing factors, manufacturing process induced parameter variations and lifetime operational-condition-dependent transistor aging are two major hurdles limiting the reliability of analog circuits. Process variations mainly influence the parametric yield value of the fresh circuits, while transistor aging due to physical effects, such as Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI), will cause another yield loss during circuit lifetime. In the past decades, the two issues were mainly studied separately by various communities, but analog designers nowadays need an accurate yet efficient method to analyze and optimize their circuits during the design phase, to ensure a more robust design tolerant of such joint effects.

This paper proposes an efficient method for sizing of analog circuits for reliability. It is based on the analysis and optimization of the fresh worst-case distance value for each circuit performance, which can be used to characterize the robustness of circuits considering process variations and aging effects in terms of *x*-sigma. The fresh and aged sizing rules as well as the maximum area constraints are checked during the optimization. The trade-off between the circuit lifetime and the price we pay in terms of layout area is studied in detail. According to the result of this trade-off analysis, a longer circuit lifetime requires more total area to be spent in layout, and designers can ensure the circuit robustness with certain layout area consumption.

1. Introduction

The continuous scaling of semiconductor technology into nanometer scale contributes to higher chip densities, improved circuit performances, lower cost per transistor, as well as several challenges and side effects, which will limit the product yield value after manufacturing and in circuit lifetime. Among those hazards, influential problems arise from manufacturing process variations and transistor degradation-related lifetime circuit reliability. These have been the major concern for both circuit design and chip manufacturing communities for decades, since these will result in parametric yield loss, early wear-out, and extra redesign costs [1].

Most of the past works quantify the influences of process variations and lifetime degradations separately. The analysis and optimization of analog circuits considering process variations alone have been in research for decades, and certain design centering algorithms and commercial software are available to achieve a design for yield (more specifically, fresh yield) [2,3]. On the other hand, the modeling of device parameter degradations such as NBTI and HCI has been so far focusing mainly on the nominal values without considering the underlying variations during manufacture process [4,5]. Solutions towards transistor aging effects alone include initial over-design of gate size [6], adding additional monitor circuitry [7], adaptive body biasing scheme [8], etc.

The reliability problem gets even worse if the joint effects of both process variations and transistor aging are considered, since they co-exist in reality both spatially across wafers and temporally over operational time. An example is illustrated in Fig. 1, where 300 Monte-Carlo simulations are run on a fresh and 5-year-old Miller amplifier with a current industrial technology. Values of Gain-Bandwidth Product (GBW) and DC Gain are shown, both moving towards negative directions. Such shifts of performance distribution result from drifts of transistor parameters, such as v_{th}, due to NBTI and HCI. Certain samples of the circuits fall out of the possible performance specifications during operational time, resulting in an early wear-out, or in other words, a shorter lifetime than expected.

It is only since recent years that the joint effects of process variations and parameter aging are considered. Authors in [9] propose an aging-aware statistical timing analysis framework for digital circuits and perform a gate sizing algorithm based on the criticality of the gate during aging. The influence of variations of NBTI itself is further studied in [10]. For analog circuits, authors in [11] present a simulation framework considering the joint effects based on a response surface model of the circuit behavior. While the

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doi:10.1016/j.microrel.2011.09.026

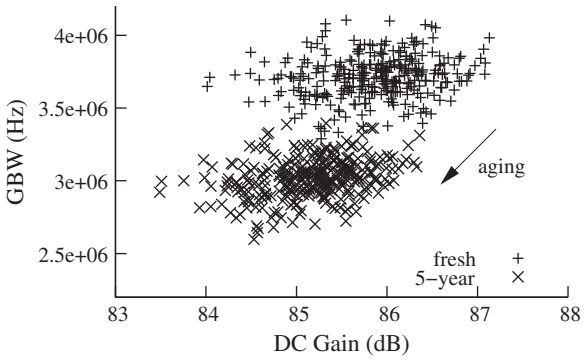

Fig. 1. Shift of the performance distribution from 300 Monte-Carlo simulation samples on a fresh and 5-year-old Miller amplifier.

framework can identify those critical parameters on the circuit reliability, a quantified solution is not available which is needed for analog circuit sizing. Authors in [12] propose a two-step optimization flow to analyze and optimize the aged yield value of the analog circuits. While the idea of [12] is simple, it is very time-consuming since another step of aged yield optimization is needed on top of the traditional fresh yield optimization process.

This paper proposes an efficient method for sizing of analog circuits for reliability. It is based on the analysis and optimization of the fresh worst-case distance value for each circuit performance, which can be used to characterize the robustness of circuits considering process variations and aging effects in terms of x-sigma. The trade-off between the circuit lifetime and the price we pay in terms of layout area is studied in detail. According to the result of this trade-off analysis, a longer circuit lifetime requires more total area to be spent in layout, and designers can ensure the circuit robustness with certain layout area consumption.

2. Process variations and transistor degradation

The variations induced during the manufacturing process can be both systematic and random [2]. Systematic variations, or intra-die variations, refer to those variations occurring repeatedly over many chips or wafers, i.e., at system level. Examples of systematic variations can be wafer-level variations due to layout-induced strain, optical-proximity correction [13], the rapid ramp-rate of the lamp thermal annealing process [14], etc. Random variations or inter-die variations, on the other hand, refer to the fluctuations which happen in a statistical manner during manufacturing process and contribute to the variations of v_{th}, t_{ox}, etc. Examples of random variations can be random discrete doping, line-edge roughness, line-width roughness, interface roughness [13], etc. In comparison to the systematic variations which can be addressed either by making changes to the design or by improvements in the manufacturing process, the random variations can only be tolerated if the initial design has enough margins built by the designers [2].

Transistor aging due to NBTI and HCI, on the other hand, happens in the time domain. These temporal aging effects shift certain transistor parameters, such as v_{th}, during the circuit's operational lifetime. The resulting circuit performances, such as delay time for a logic gate path or dc gain for an operational amplifier, will drift from their respective initial fresh values. Since for semiconductor industry, there exists an expected circuit lifetime for different product categories, such performance degradation due to transistor aging may cause an early wear-out of the circuit before the end of the expected lifetime.

Taking into account the above two joint effects, designers have to consider early during the design phase the worst case scenario that can happen during manufacturing process and operational lifetime, such that certain weak points can be detected early, and additional safe margins can be assigned, to ensure that the circuit can work properly under process variations and transistor aging.

3. Fresh yield and aged yield

The parametric yield value of the fresh circuits is called fresh yield [12]. It refers to the percentage of products after manufacturing which can satisfy all of the pre-defined performance specifications. If we define the transistor parameters that have a statistical distribution during the manufacturing process as statistical parameters $s \in R^{n_s}$, where n_s is the number of statistical parameters, then there exists an acceptance region A_s in the statistical parameter space, which refers to the part of the statistical distribution that can satisfy the performance boundaries for various operating conditions:

$$A_s = \left\{ s \middle| \underset{\theta \in \Theta}{\forall} f_L \leqslant f \leqslant f_U \right\} \tag{1}$$

where f_L and f_U refer to the lower and upper bounds for the performances $f \in R^{n_f}$, and $\theta \in R^{n_\theta}$ refers to the operational parameters such as supply voltage, temperature of the circuit.

The statistical parameters are usually modeled by Gaussian, log-normal or uniform distributions. Without loss of generality, those distributions can be transformed into a Gaussian distribution with a nominal vector s_0 and covariance matrix $\boldsymbol{C}$ as: $s \sim N(s_0, \boldsymbol{C})$ [15], whose probability density function (pdf) is

$$\mathrm{pdf}(s) = \frac{1}{\sqrt{2\pi}^{n_s}\sqrt{\det \boldsymbol{C}}} \cdot \exp\left(-\frac{\beta^2(s)}{2}\right) \tag{2}$$

The ellipsoids shown in Fig. 2 are the level contours of the two-dimensional Gaussian distributed statistical parameters. These ellipsoids are denoted as $\beta^2(s)$ in (2), which can be formulated as

$$\beta^2(s) = (s - s_0)^T \cdot \boldsymbol{C}^{-1} \cdot (s - s_0) \tag{3}$$

The fresh yield value Y thus can be formulated as

$$Y = \mathrm{prob}\{ \underset{\theta \in \Theta}{\forall} s \in A_s \} \tag{4}$$

which is equivalent to the integration of pdf of s in A_s:

$$Y = \int \cdots \int_{s \in A_s} \mathrm{pdf}(s)\mathrm{d}s \tag{5}$$

When transistor aging effects are considered on top of the manufacturing process variations, the aged yield value $Y(t)$ at time t corresponds to the percentage of the circuits which still can satisfy all of the performance specifications. Since the original distribution around $s_0(t_0)$ will shift to a new distribution, a certain percentage of the fresh circuits which satisfied the specification will fall out of the acceptance region at t_1, as can be seen in Fig. 2.

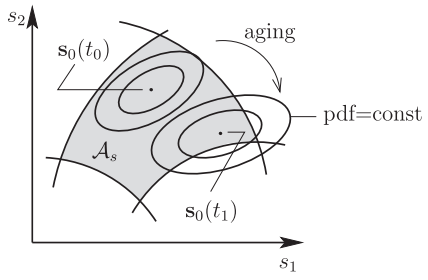

Fig. 2. Shift of statistical parameter distribution from t_0 to t_1 as a result of aging in the space of statistical parameters. A_s refers to the acceptance region closed by four performance boundaries in this example.