

Efficient damage sensitivity analysis of advanced Cu/low- k bond pad structures by means of the area release energy criterion

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Abstract

For integrated circuit (IC) wafer back-end development, state-of-the-art CMOS-technologies have to be developed and robust bond pad structures have to be designed in order to guarantee both functionality and reliability during waferfab processes, packaging, qualification tests, and, of course, usage. It is now well established that for future CMOS-technologies (CMOS065 and beyond), low- k dielectric materials will be integrated in the back-end structures. However, bad thermal and mechanical integrity as well as weak interfacial adhesion result in major thermo-mechanical reliability issues. Especially the forces resulting from packaging related processes such as dicing, wire bonding, bumping and molding are critical and can easily induce cracking, delamination and chipping of the IC back-end structure when no appropriate precautions are taken. This paper presents an efficient method to describe the damage sensitivity of three-dimensional multi-layered structures. The index that characterizes this failure sensitivity is an energy measure called the Area Release Energy, which predicts the amount of energy that is released upon crack initiation at an arbitrary position along an interface. The benefits of the method are: (1) the criterion can be used as damage sensitivity indicator for complex three-dimensional structures; (2) the criterion is energy-based, thus more accurate than stress-based criteria; (3) unlike recent fracture mechanics approaches, no initial defect size and location has to be assumed a priori. A mesh objectivity condition is formulated resulting from numerical experiments. The method is applied to advanced IC back-end structures, revealing not only the most critical back-end design but also the critical interfaces in the bond pad structures at which delamination might occur. In order to bridge the length scale difference between the wafer level and the back-end structures, a multi-scale method has been implemented in the finite element code MSC.Marc. In this way, effects of e.g., packaging and wire bond loading at the global level can be studied while taking into account the possibility of occurring failure phenomena at the local, back-end level. The validity and applicability of the method will be demonstrated by considering several Cu/low- k back-end structures. The obtained results are in good agreement with experimental observations.

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1. Introduction

Due to the reduced design margins and shorter time-to-market in IC back-end process development, trail-and-error approaches are not sufficient anymore and a more

sophisticated methodology based on numerical simulation and optimization techniques is required. With this virtual prototyping and qualification methodology thermo-mechanical reliability issues are already included in the design phase rendering proposed design changes more efficient and thus cheaper. It is now well established that for future CMOS-technologies (CMOS065 and beyond), low- k dielectric materials will be integrated in the back-end structures [1]. The thermo-mechanical reliability of bond pads due to the bad thermal and mechanical integrity of

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the low- k materials and associated interfaces, is still an important issue in the development of new Cu/low- k CMOS-technologies [2]. The resulting forces due to the wire bonding process, qualification tests and packaging processes can easily result in reliability problems like bond pad delamination and low- k cracking. However, bad thermal and mechanical integrity as well as weak interfacial adhesion result in major thermo-mechanical reliability issues. Especially the forces resulting from packaging related processes such as dicing, wire bonding, bumping and molding are critical and can easily induce cracking, delamination and chipping of the IC back-end structure when no appropriate precautions are taken [3].

An important qualification test for wire integrity is the wire pull test. The typical configuration of this wire pull qualification test, where the wire is pulled by a hook, is visualized in Fig. 1a. The wire and the bond pad structures should withstand a certain force level before failure of the wire or the bonds occurs. Actually, two failure modes are possible: metal peel off and neck break, as illustrated in Fig. 1b. While the neck break failure mode is acceptable, the metal peel off mode (prior to neck break) is unacceptable as the occurring delamination in the back-end structures indicates that the integrity of the bond pad designs is not sufficient. An example of actual bond pad delamination of a CMOS90 Cu/low- k process due to this wire pull qualification is given in Fig. 2.

The thermo-mechanical reliability of the (low- k) bond pads depends strongly on the underlying metal and via lay-

out of the back-end layers. The copper metal lines and vias act as mechanical support in the relatively weak low- k matrix. Due to the complex interaction of multiple processes, materials and interfaces, however, an optimum metal layout design is difficult to lay out on beforehand. In order to rank the structural integrity of different bond pad designs, finite element analyses will be used allowing optimization of the bond pad structure in the design phase. The developed methodology is based on a three-dimensional multi-scale sub-modeling approach similar to Wang et al. [4]. However, in our paper, a dedicated homogenization procedure has been developed resulting in equivalent, fully anisotropic stiffness properties representing the mechanical behavior of the back-end structures at the global, packaging level. As a result, the displacements at the global level are calculated more accurately, compared with the approach proposed in [4]. Next, the so-called localization step permits to determine local field variables by using the global displacement solution field [5]. At both levels, the Area Release Energy (ARE), described in [6], will be calculated as failure criterion. More specifically, the amount of energy is calculated that is released upon delamination of an area of predefined size for any position along any interface without the need of an initial crack. The ARE value indicates the risk of delamination of the interfaces without knowing a priori the exact location of possible failure(s). This method will be used to study the damage sensitivity of several three-dimensional bond pad structures. The obtained results will be validated with experimental observations.

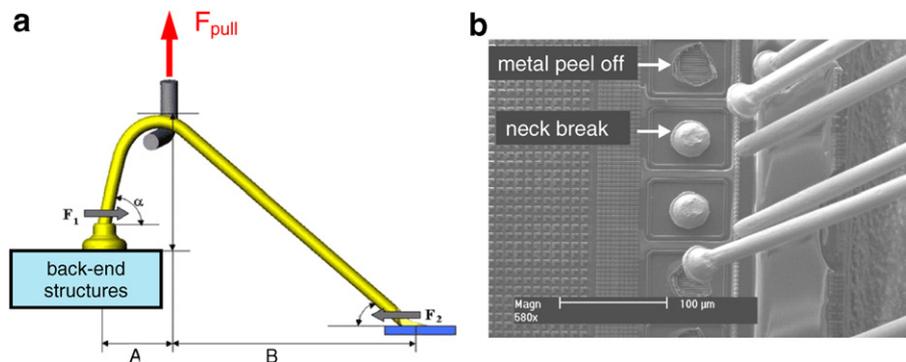


Fig. 1. Schematic of the wire pull test.

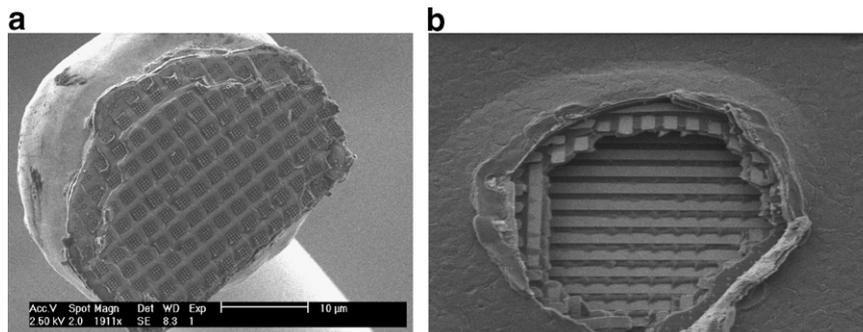


Fig. 2. Examples of bond pad delamination due to wire pull testing.

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