Microelectronics Reliability 53 (2013) 1311–1314

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

SEL-UP: A CAD tool for the sensitivity analysis of radiation-induced Single Event Latch-Up

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ARTICLE INFO

Article history:
Received 11 June 2013
Received in revised form 24 July 2013
Accepted 24 July 2013

ABSTRACT

Space missions require extremely high reliable components that must guarantee correct functionality without incurring in catastrophic effects. When electronic devices are adopted in space applications, radiation hardened technology should be mandatorily adopted. In this paper we propose a novel method for analyzing the sensitivity with respect to Single Event Latch-up (SEL) in radiation hardened technology. Experimental results obtained comparing heavy-ion beam campaign demonstrated the feasibility of the proposed solution.

1. Introduction

Single Event Effects (SEEs) is a widely known phenomenon that leads to permanent or temporary damage due to heavy ion exposure. With the progressive scaling to smaller technologies, there is an increasing concern that circuits may be more susceptible to various mechanisms including Single Event Latch-up (SEL), Single Event Burnout (SEB) or Single Event Gate Rupture (SEGR). In particular, the occurrence of SEL events happens when a parasitic NPNP feedback latch structure becomes biased into the on state due to a very dense track of electron–hole pairs which are created along the heavy ion track through the silicon [1]. This latch-up is self-maintained since there is a positive feedback path which sustains it and that requires an external power cycle in order to be deactivated [2].

The evaluation of permanent faults generation in modern Integrated Circuits (ICs) is of fundamental importance for several application fields. Environmental noises may generally provoke the generation of soft-errors, that temporarily affect the operational life of the electronic system but that can be corrected using the adequate countermeasures. Vice versa, permanent faults does not allow the electronic systems to be recovered, and if not preventively developed, the permanent fault affected electronic system may be definitively broken.

When safety critical applications, such as space, avionics or rail transport, are considered, statistics data indicates that a range between 10% and 40% of the whole faults may possibly turn into permanent fault generating a short on the power of the system [3]. It is therefore mandatory to adopt effective methodology to measure and subsequently protect electronic system versus permanent faults.

When a particle crosses a silicon junction, a coulombic interaction between the particle and the electrons is generated. This effect is common for all charged particles. When a charged particle traverses the silicon area, it loses energy through atoms ionization and excitation. The moving charged particle induce electromagnetic forces on atomic electrons and transfers energy to them. The energy transferred in a single electronic collision is only a small portion of the heavy charged particle energy, however through the whole traversing path, the energy can be considerably high. The energy is measured as linear rate of energy loss of a charged particle in a medium volume [4]. This quantity is extremely important in radiation physics, and it can generally be referred to with two names: stopping power or Linear Energy Transfer (LET). This quantity expresses the average energy transferred through traversing a given space of medium ($-\Delta E/\Delta x$) [5].

In this paper we describe a new computer-aided design (CAD tool) that, in conjunction with silicon layout information and circuit behavioral functionality is able to depict the probability and the expected location where single event latch-up may happen and therefore to provide such kind of information to designers. From the scientific point of view, the main contribution of the present paper is to provide the complete method for the analysis and the evaluation of single event latch-up effects on integrated circuits implemented with radiation hardened technology. The main advantage of the proposed tool is the possibility to depict, once the design is in the early manufacturing stage, which is the expected SEL effect rate, and, possibly by using the feed-back provided by our tool, improve and reduce the SEL impact on the circuit. In particular, the proposed approach is able to provide an advancement in the scientific field of the measurement of the robustness of VLSI technology in safety–critical environment, since we provide the

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0026-2714/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.microrel.2013.07.104

first tool able to predict the location and the probability of SEL effects giving the information related to the physical layout and to the electrical stimulus applied.

The proposed method has been validated through comparison with high temperature radiation test analysis of the SEL sensitiveness of MG2 Atmel radiation hardened technology [6]. The tests have been performed with heavy ion at the GANIL facility, Caen, France. Thanks to the radiation experiment, we compared the result provided by the developed sensitivity analyzer tool and we obtained a full compliance between them, thus demonstrating the effectiveness of the proposed method.

2. Related works

Several documented heavy-ions SEL tests [3] demonstrated that physical damages may become worse and in some case evident with the increasing of LET and fluence. SEL test procedures are included in different official standard widely adopted to manage such kind of tests. An example of these standards is the ASTMF1192 or the EIA/JESD57. The common rules provided by the standards is that SEL test must be performed at the maximum Device Under Test (DUT) datasheet voltage and temperature and applying a fluence greater than 1E7 ions/cm^2[7].

Although recent investigations have been focused on nanometer technologies showing effects of temperature and angle of incidence for heavy ions on latch-up effects [8] and they demonstrated that latch-up cross-sections increase with both increase of temperature and incident angle, the usage of micrometer technologies such as 0.5 urn is still largely used in space avionic systems and nowadays, a wide set of communication and other satellite systems are currently adopting it [9]. The results provided by tests of this technology under severe conditions evaluating its behavior, enable the adoption of rad-hard technology in a wider set of application fields including satellite systems working in extreme temperature and harsh environments [10]. The analysis and measurement of faults effects on digital Integrated Circuits is becoming more and more relevant as demonstrated by several previous studies on the field [11].

3. The proposed analysis tool

The main purpose of the sensitivity analyzer tool (also called *SEL-UP)* is to provide an early evidence of the circuit sensitive area before to implementing the circuit on the real integrated circuits and manufacture the correspondent ASIC device. The flow of the tool is illustrated in Fig. 1.

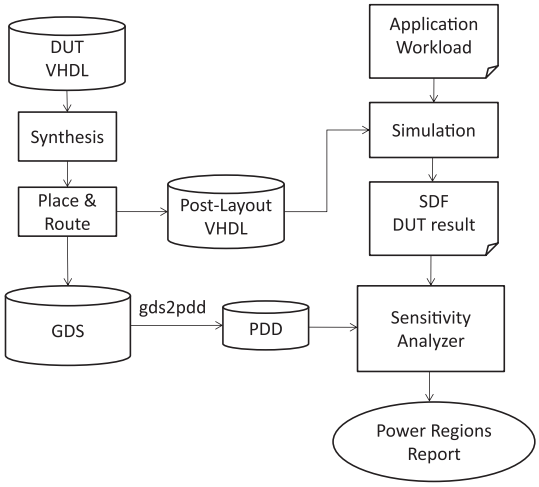

Fig. 1. The flow of the developed SEL-UP tool.

The tool consists of two flows: one related to the hardware circuit description and the other related to the application executed on the circuit. The first flow starts from the VLSI Hardware Description Language (VHDL) of the Design Under Test (DUT) which is synthesized and implemented through place and route algorithm on the selected technology. The results of the place and route implementation algorithms provide two different files: a post-layout HDL description and a Graphic Database System (GDS) Format. This format is generally used to describe the implementation of a circuit considering its layout characteristics. This format allows accurately describing VLSI placement and routing at a physical design level of an electronic circuit. A GDS file locates cells over the circuit core region representing the placement locations and including timing-related information both related to logic gates and interconnections as well as geometric layout information. The format is standardized in order to provide a common circuit netlist and topology format which can be easily used to provide layout statistics along with a list of placement locations of each circuit logic cells. The GDS description file is then converted into a Physical Design Description (PDD) which is a proprietary file format which describes the design logic resources in a graph-based format organization.

Vice versa, the analysis flows related to the executed application is based on the simulation of the post-layout VHDL description generated by the implementation tools. The simulation is performed applying to the circuit the input stimuli related to the application workload defined by the user. The simulation provides as a result a timing annotated post-layout simulation in a Synchronous Data Flow (SDF) format which contains the signal switching activity related to each routing segment and to each logic gate. Once the PDD circuit database and the SDF simulation results are generated the SEL-UP tool is executed.

The SEL-UP tool has been implemented as a software tool, able to evaluate the distribution of the single event latch-up location along with the physical layout of the circuit under test. It is capable to generate a profile of the sensitivity regions inside of the circuit layout and on the basis of the applied patterns, to individuate which region or detailed location is the most sensitive and critical with respect to the radiation beam characteristics.

The main idea of the algorithm is based on the current absorption measurement estimation of each logic element of circuit, considering the physical characteristics of the implemented circuit, obtained by analyzing the layout masking layers and the logic element details, such as fan-in and fan-out signals connected to each logic gate and the respective logic cone position inside of the integrated circuit array. The Single Event Latch-Up (SEL) metric is computed for each clock cycle of the provided SDF simulation report and it is calculated for each clock cycle transition. The generated sensitivity region metric allows effectively estimating the current absorption of the circuit in relation to the logic gate position therefore providing a profile of the current absorption in the different portions of the circuit depending on the application workload applied to the circuit. The results of the sensitivity analyzer tool is then provided into a power regions report that provides to the final user a detailed perspective of the current absorption of the circuit depending on the instance of time of the executed application. Thanks to the analysis of the current graph consumption associated to each circuit region, it is possible to identify the progressive variation of the current absorption along with the modification of the user application. The result of the sensitivity analyzer phase is fundamental in order to depict the data obtained by the measurement of latch-up errors during the radiation experiment analysis since it is fundamental to identify a correlation between the absorption of the current with respect to the identified temporary or permanent errors.