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# The time-delay digital tanlock loop: performance analysis in additive Gaussian noise

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**Abstract**

Recently, a new non-uniform sampling digital phase-locked loop, the time-delay digital tanlock loop (TDTL), has been proposed. We have analyzed in a previous work the first- and second-order TDTLs under noise-free conditions. In this work, we analyze the performance of the TDTL in the presence of additive Gaussian noise for different values of the loop parameters. It is shown that the expected value of the steady-state phase errors at the input and the output of the phase error detector are equal to the noise-free steady-state values, while the variance is significantly reduced when the signal-to-noise ratio is increased or the phase shift introduced by the time-delay approaches 90°. The locking ranges of the TDTL parameters under noise-free conditions are unchanged by the presence of noise. 

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## 1. Introduction

Phase-locked loops (PLLs) are important subsystems in signal processing and communications. They contribute significantly to communications where they are

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widely used in synchronization, frequency modulation, frequency tracking and demodulation. PLLs have a variety of applications in signal processing like filtering, frequency synthesis, signal detection, motor-speed control and many other applications [1]. Digital signal processing has dominated over analog signal processing due to the increasing performance, speed, reliability and the great reduction in size and cost of digital integrated circuits, also motivated by the huge developments in microprocessor technology. Consequently, digital phase-locked loops (DPLLs) have dominated over the analog PLLs as they solved many problems associated with the analog loops like sensitivity to dc drifts and the need for initial calibration and periodic adjustments. Nonuniform sampling DPLLs have been proved to be the most important digital phase-locked loops because they are simple to implement and easy to model [2]. Significant advantages over other nonuniform sampling digital phase-locked loops have been obtained by the digital tanlock loop (DTL), proposed in [3]. The first-order DTL has wider locking range than other nonuniform sampling DPLLs. Locking conditions of DTL are unaffected by the variation of the input signal power under noise-free conditions, hence no need for automatic gain control, and they have reduced sensitivity to this variation in the presence of noise [3]. DTL proved to be efficient for many applications in digital communications (see, for example, [4,5]). The constant $90^\circ$ phase-shifter is a vital part of DTL and all its modifications (see, for instance, [6,7]), which can be implemented using a Hilbert transformer [8,9]. However, a digital Hilbert transformer introduces approximations and imposes limitations on the range of input frequencies, especially when implemented on a microprocessor [8,9].

In [10,11], a constant time-delay unit is used to produce a phase-shifted version of the incoming signal, giving rise to the time-delay digital tanlock loop (TDTL). This method reduces the complexity of the phase-shifter and avoids the limitations and other problems that accompanies the $90^\circ$ phase-shifter in the conventional DTL (CDTL).

Except for the linearity of the characteristic function of the phase error detector, the main advantages of CDTL are maintained by TDTL despite its reduced structure. First, under noise-free conditions its performance is not affected by the variation of signal power. Second, the first-order loop can have wider locking range than other sinusoidal DPLLs (including CDTL) if the circuit parameters are properly chosen. The region of locking independently of initial phase errors in the first-order loop can be made larger than that of the first-order CDTL since the conditions of independent locking are less stringent in TDTL as a result of nonlinearity.

Although the locking range of the second-order TDTL is reduced compared to that of CDTL, this reduction is not a severe shortcoming since it mainly concerns high values of the loop gain $K_1$ which are not desired in the presence of noise. In fact, any range of input frequencies can be handled after a suitable arrangement of the circuit parameters.

In this paper, we analyze the performance of the first and second-order TDTLs in the presence of additive Gaussian noise (parts of this work appeared in [12]). It is shown that, in the presence of additive Gaussian noise, the phase at the output of the