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Performance analysis of all optical NOR gate at 80 Gb/s

Rekha Mehra [a,*], Shikha Jaiswal [b], H.K. Dixit [c], Pallavi Singh [c]

[a] Department of Electronics and Communication, Government Engineering College Ajmer, N.H. 8, Beawar – Jaipur Bypass, Barliya Circle, Ajmer, India
[b] Department of Physics, SDPG College, Muzaffarnagar: (C.C.S. University, Meerut), India
[c] Department of Electronics and Communication, University of Allahabad – 211002, India

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ABSTRACT

In this paper an 'all optical NOR gate' based on four wave mixing in Semiconductor Optical Amplifier is proposed. The performance of this NOR gate is good and satisfactory up to 100 Gbit/s. The extinction ratio and the maximum output power are optimized by appropriate choice of design parameters of SOA and the maximum extinction ratio 10.8 for this design has been obtained at 80 Gbit/s. Unlike the related research papers referred, this paper highlights both power level and time domain analysis of the proposed NOR gate.

1. Introduction

Optical computing devices are evolving rapidly to satisfy the needs of the new broadband network, which is characterized by the diversified use of Internet and other multimedia applications. Optical computing devices include uses of wavelength conversion, demultiplexing, regeneration and storage techniques, etc., which will play a major role in the development of ultra-high speed optical network. The backbone of all these devices is all optical logic gates. All Boolean logic gates can be implemented using universal logic gates NOR and NAND gate. This paper describes design and performance analysis of all optical NOR gate using four wave mixing, third order non linearity in SOA. A characteristic feature of this nonlinear phenomenon is that it is very fast for the rise time; however, there is slow recovery corresponding to the band-to-band carrier recombination lifetime. This slow recovery response is filtered out by the wave length filter followed by SOA. Whenever FWM is generated in SOA, carrier signal, i.e. probe signal power will be distributed among the four waves and hence output will correspond to '0' logic level otherwise carrier at the output will have high power corresponding to level '1'.

2. Principle of operation

The optical NOR gate in this proposed design consists of two couplers and SOA followed by the band pass filter as shown in Fig. 1. Two data bits A & B generated by bit sequence generator are used to generate Gaussian pulses corresponding to the input bits. These pulses are fed to the first coupler which will generate the logic OR gate, therefore the output will be high when any of input is high. This output is coupled with the probe signal by the second coupler and the output of 2nd coupler is fed to SOA. Thus three signals (two data and one probe) are given at the input of SOA. According to the property of SOA, when any two signals out of the three will be high, FWM will be generated, and carrier signal, i.e. probe signal power will be distributed among these four waves. Therefore, when the probe signal will be received after the band pass filter, it will reflect zero logic, thus low power output will be received. On the contrary, when both the inputs A & B are zero, no FWM will be generated and probe signal at the output of the filter will have high power. This will reflect high logic, i.e. '1' output. Thus the complete design will work as logic NOR gate. The observations for NOR gate has been verified up to 100 Gbit/s, by setting the upper threshold level for zero logic at 19 dBm.

As mentioned above the main technique behind this logic gate design is FWM generation in SOA. In switching devices, using SOA, population inversion is realized by current injection. When an intense gate pulse is applied at the input of SOA, it causes gain saturation and an associated refractive index change takes place. This is the 3rd order nonlinear process. A characteristic feature of this response is that it is very fast for the rise time; however, there is slow recovery corresponding to the band-to-band carrier recombination lifetime and is of the order of 100 ps–1 ns [1,2].

This slow component has been the obstacle in realizing ultra-fast switching devices above 100 Gbit/s. There are two methods for solving this problem. One is to use a wave length filter to select only the very fast component. Another method is to cancel out the

* Corresponding author.
E-mail addresses: mehra_rekha@rediffmail.com (R. Mehra), shikhajk@gmail.com (S. Jaiswal), hkdxit@gmail.com (H.K. Dixit).

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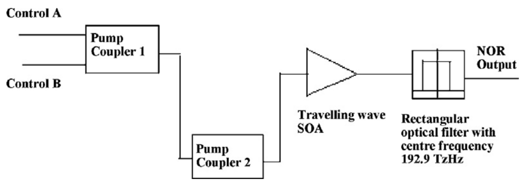

Fig. 1. The experimental setup for all optical NOR gate.

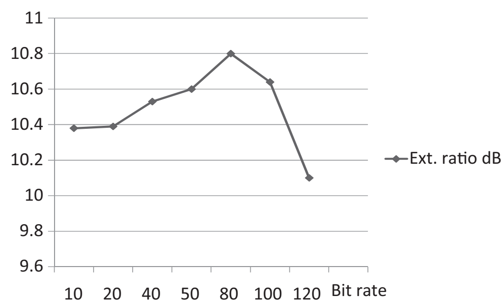

Fig. 2. Variation of extinction ratio with bit rate.

Table 1
Truth table for NOR gate at 80 Gbit/s.

Input A	Input B	Output level (power in dBm)
0	0	1 (27.797)
0	1	0 (15.641)
1	0	0 (16.997)
1	1	0 (16.239)

slow response component by using MZI with SOA, i.e. placing SOA in the arms of MZI. In the proposed design of NOR gate the filter method has been adopted. Basic concept of the design has been taken from the book titled 'Ultrafast All Optical Signal Processing Devices' [1]. The same concept has been mentioned [3]. However, this paper does not include the design and mathematical analysis, only the concept has been mentioned through the block diagram. Ali Hamie et al. in their paper 'All optical logic NOR gate using two-cascaded semiconductor optical amplifiers' [5] have proposed the design of NOR gate using two-cascaded semiconductor amplifiers. This configuration uses the gain nonlinearity due to the mutual gain modulation of the two SOAs. Their design uses cross gain modulation in SOA with counter propagating operation. In our proposed design we have used four wave mixing in SOA and the design uses single SOA, while the design mentioned in [5] uses two SOAs for NOR gate. Four wave mixing method has the main advantage over cross gain modulation based method that it is independent of modulation format. The gain of SOA can respond to very fast fluctuations in optical signal and hence can be used for higher bit rate of operation [4]. Another method uses the polarization states to identify logic '1' and '0'.This method uses polarization controller at the input to change the input polarization states and at the output to adjust the polarization state. Result wise both the methods can be put in parallel although the circuit used for polarization based method is more complex.

3. Simulation and results

Proposed NOR gate as discussed above will have two control inputs A and B which will be kept 0 or 1 by setting bit in bit sequence generator. Whenever input bit is '1' it will generate Gaussian pulse at the output of Gaussian pulse generator. Output of the NOR gate will be at carrier frequency, i.e. probe signal frequency used.

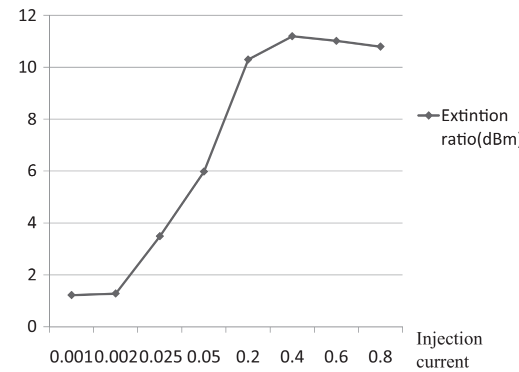

Fig. 3. Variation of extinction ratio with input injection current to SOA.

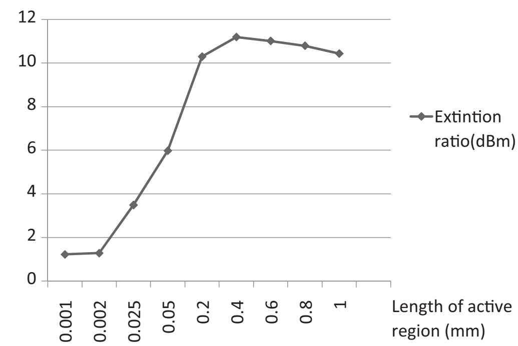

Fig. 4. Variation of extinction ratio with length of active region.

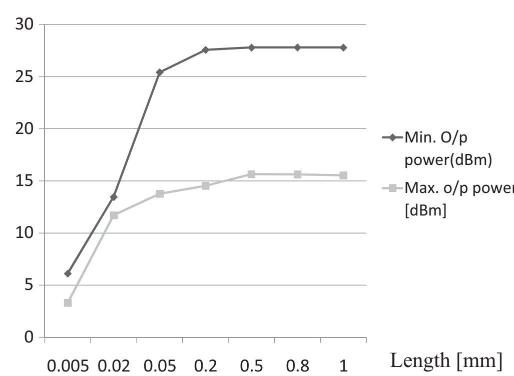

Fig. 5. Variation of minimum and maximum output (for level '1' and '0') with length of active region of SOA.

Table 2
Variation of minimum and maximum output power for level '1' and '0' with length of active region of SOA.

Length (mm)	Min. output power (dBm)	Max. output power (dBm)
0.005	6.11	13.730
0.02	13.46	17.509
0.05	25.42	17.943
0.2	27.57	18.304
0.5	27.79	16.997
0.8	27.80	16.981
1.0	27.79	16.890

Observations of the gate output have been taken from 10 to 120 Gbit/s. The performance/truth table of NOR gate at different bit rates are evaluated and the same at 80 Gbit/s is mentioned here in Table 1. Satisfactory results are obtained up to 100 Gb/s with the variation in power level for logic '1' from 27.807 dBm at 10 Gb/s to 27.794 dBm at 100 Gb/s and for logic '0' from max. 17.429 dBm