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Reconstruction and thermal performance analysis of die-bonding filling states for high-power light-emitting diode devices

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HIGHLIGHTS

- Precise die-bonding thermal paths were reconstructed on X-ray transmission images.
- The filling states of bonding materials were taken into consideration in our models.
- The temperature uniformity was analyzed in chip-scale with hotspots located.
- The reconstructed model is a method to predict the LED performance accurately.

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ABSTRACT

This paper proposed a half-experimental model to reconstruct the die-bonding thermal path of high-power light-emitting diodes (HP-LEDs). In this model, the partially insufficient filling of bonding materials and their directional/random distributions ("filling state" for short) have been taken into consideration. Both the silver-paste structure and the Au/Sn-eutectic structure were analyzed and compared. Finite element analysis (FEA) indicated that qualified die-bonding with uniform filled areas would lead to much better thermal performance. Hotspots have been observed above the insufficiently filled regions. The simulated thermal resistances of the defective bonding were 5.4 times and 2.1 times higher than those of the qualified samples under conditions of Au/Sn-eutectic and silver-paste, respectively. Transient thermal resistance measurements further demonstrated that the devices with different filling states would result in distinct thermal resistances. Interestingly, it was noted that although the qualified silver-paste bonding had a larger filled area, the measured thermal resistance remained higher than that of the defective Au/Sn-eutectic bonding because of the high contact thermal resistance caused by poor wetting properties. Furthermore, defectively bonded LED devices revealed a poor maintenance of luminous flux after 500 h of aging, which was consistent with the results of thermal performance analysis on the reconstructed die-bonding models.

1. Introduction

With the development of high-power light-emitting diodes (HP-LEDs) [1,2], the move to replace general lighting fixtures with solid-state lights (SSLs) has become widespread. To reduce the cost of the rebuilding investment of lighting systems, the power density of LED chips is becoming increasingly higher, reaching a value of 125A/cm^2 in the latest Cree® products [3]. This continuously increasing injection current has led to remarkable heat generation in the active layer of LEDs, and overheated p–n junctions have led to a decrease in luminosity [4,5], as well as premature failure after aging [6–8]. Therefore, thermal management has become one of the most important issues with respect to energy efficiency and reliability. In practice, LEDs are manufactured into single components or compact chip-on-board (COB) packaged devices. Regarding the former, a surface mounting assembly of components on metal-core print circuit boards (MCPCBs) is necessary. This assembly introduces several sources of thermal impedance into lighting systems. COB packaged devices have been reported as an effective solution to this problem, exhibiting a significantly lower thermal resistance by reducing the distance of the thermal path [9,10]. In both cases, LED chips are inevitably die-bonded to a large leadframe substrate with high thermal conductivity by using a layer of bonding material.

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Nomenclature

A	surface/cross-sectional area [mm^2]
C_p	specific heat [J/(kg K)]
F	view factor
P	pressure [Pa]
q	heat flow [W]
$\dot{q}$	heat flux [W/m^2]
R	thermal resistance
T	temperature [K]
u	x-component of velocity [m/s]
v	y-component of velocity [m/s]
ω	z-component of velocity [m/s]

Greek symbols

γ	reflectivity
δ	thickness [μm]
ε	emissivity
λ	thermal conductivity [W/(m K)]
μ	dynamic viscosity [N/m^2s]
ρ	density [kg/m^3]
σ	Boltzmann's constant

Subscripts

atm	atmosphere
bond	die-bonding layer
c	chip
e	element
Gan	gallium nitride
i	the surface i
j	the surface j
l	leadframe substrate
out	emit out
∞	ambient

Moreover, from the optical point of view, a roughened leadframe substrate was preferred for improving light extraction [11,12]. Therefore, it is easily understood that it was difficult to form a perfect contact with the die-bonding material [13,14]. Although die-bonding materials such as silver-paste [14,15], carbon nanotube (CNT)-embedded silver-paste [16], SAC305 solder [15–17], and Au/Sn-eutectic [14,15,18] have been studied as potential solutions, the die-bonding layer is still one of the greatest conductive barriers in the thermal path of LED devices.

The bonding layer was usually simplified as a regular contact structure in conventional design or analysis models. Thus, the thermal resistance directly calculated based on these models was much lower than the measured values [19,20]. Different mechanisms have been reported in the literature to explain such inconsistencies. From the thermal properties point of view, the die-bonding thermal resistance could be decomposed into one component representing the bulk thermal resistance and another component representing the contact thermal resistance [13,14]. Some researchers believed that the thermal conductivities of die-bonding materials were significantly lower than the theoretical values (effective thermal conductivity argument with respect to the bulk thermal resistance) [19–21]. Others have indicated that the increased thermal impedances observed were mainly caused by poor contact conditions (contact thermal resistance argument) [14]. Generally, voids exist in the die-bonding layer in the forms of top/bottom, middle, and through modes [22]. Only in the bonding layers, wherein there is a large amount of middle voids, the thermal conductivities of bonding materials would notably decrease. However, in a real LED device, the die-bonding layer is extremely thin and not too large. In addition, die-bonding materials are prepared under sufficient deaeration conditions. It is reasonable to assume that the die-bonding materials are dense. Accordingly, it is believed that the contact thermal resistance argument is the most appropriate in these cases.

T. Chung et al. calculated the thermal resistance based on an improved model with periodical stripe-like voids embedded in bonding structures, which was based on the real filled area ratio of bonding materials observed in ultrasound images [14]. Clearly, in his calculations, the material distribution was neglected, whereas in recent works, it was observed that the filling states with distinct distributions of die-bonding materials would not only affect the overall thermal resistance [22] but also create a significantly nonuniform junction temperature [23]. This paper extends the previous investigations and proposes a novel half-experimental model based on X-ray transmission images. The models are submitted to finite element analysis (FEA) as well as thermal resistance networks analysis and finally utilized to discuss the luminous properties of LED devices. This work presents a more precise method for predicting HP-LED die-bonding quality compared with other previously reported methods.

2. LED device structure specification

Vertical HP-LED chips with Si submounts were used in the experiments. Fig. 1 reveals a schematic of the components (Type 3535), which consists of a high-temperature co-sintered ceramic (HTCC) leadframe substrate with top/bottom-layer copper films, an LED chip bonded with Au/Sn-eutectic or silver-paste, a phosphor coating, and a dome-shaped silicone lens. Roughening processes were applied to the surface of the leadframe to form a diffusely reflecting surface that would significantly improve the outcoupling of rays, as shown in the FAM image of Fig. 1. The mid-pad of the leadframe was reserved as a heat-dissipating path. The Au/Sn-eutectic and silver-paste bondings were performed via reflowing and oven-curing, respectively. Fig. 2 shows the recommended reflowing temperature profile. The maximum temperature in this experiment was set to 310 °C and held for 5 s. The reflowing process was continued for 4 min. After reflowing, ultrasonic and plasma cleaning were used to remove the residual flux. For the silver-paste bonding, the components were cured in an oven at 150 °C for 2 h, and the cleaning procedure was not necessary. Also worth mentioning is that no external force was applied to the chip during reflowing or oven-curing to avoid damages on the epitaxial layer. The thermal conductivities of the materials are listed in Table 1.

3. Die-bonding thermal path reconstruction

As shown in Fig. 3, the Au/Sn-eutectic-bonded samples exhibits a better appearance than those bonded with silver-paste. The bonding material was extruded from the side wall in the latter case because the thickness of the silver-paste bonding layer was up to 7.5 μm, considerably larger than that of the Au/Sn-eutectic bonding layer which was only 3 μm. Fig. 4(a) shows typical X-ray transmission images of the two die-bonding structures