Expert Systems with Applications 42 (2015) 6658–6673

Contents lists available at ScienceDirect

Expert Systems with Applications

journal homepage: www.elsevier.com/locate/eswa

A scalable accuracy fuzzy logic controller on FPGA

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ARTICLE INFO

Article history:
Available online 29 April 2015

Keywords:
Scalable
Fuzzy accuracy factor
Fuzzy logic controller (FLC)
FPGA

ABSTRACT

A distributed, scalable and flexible fuzzy logic controller (FLC) without increasing additional hardware cost by fuzzy accuracy factor is proposed. In order to improve fuzzy logic operation speed, multi-input/multi-output (MIMO) fuzzy system is decomposed into several independent two-input/single-output (TISO) subsystems in parallel. The decomposed TISO FLC can deal with scalable requirements in terms of number of input language variables, output language variables, data accuracy types and fuzzy rules. In this paper, the systematic design methods are presented in detail, and the scalable TISO FLC architectures are addressed with fuzzification of fuzzy accuracy factor and analog-to-digital conversion (ADC) quantizer, fuzzy rules and fuzzy inference engine, and the defuzzification by a scalable divider. At last, A JTAG-TCL tool is developed to compare the scalable TISO FLC with other FLCs in resource, accuracy, and speed. The experiment results of photovoltaic (PV) system indicate that the proposed FLC has flexible control accuracy, fast response and better tracking performance.

1. Introduction

Since L. A. Zadeh firstly proposed the statement of fuzzy set theory in 1965, Fuzzy logic controllers (FLCs) that can imitate operation behavior of human experts have been used in many application fields. The success of FLCs is mainly due to their ability to cope with knowledge represented in a linguistic form instead of representation in the conventional mathematical framework (Monmasson & Cirstea, 2007).

According to the application targets, FLCs can be divided into two classes: general-purpose fuzzy processor with specialized fuzzy computations and dedicated fuzzy hardware for specific applications (Kim, 2000). The general-purpose fuzzy processor has an advantage of flexibility with lower efficiency, while the dedicated fuzzy hardware has high calculation speed with some limits. Therefore, a FLC is expected to integrate their advantages of both flexibility and high speed. The approach to implement fuzzy logic systems can be software-only, hardware-only, or a combination of software and hardware (Salcic, 2001). From implementation of technology package, FLCs can be integrated in FPGA or application specific integrated circuit (ASIC) chip. ASIC hardware has longer research and development cycle and higher cost than FPGA. FPGA is suitably adopted to implement field-oriented mechanism and developed control algorithms for possible, low-cost, and high-performance industrial applications (Kim, 2000; Monmasson & Cirstea, 2007; Rani, Kanagasabapathy, & Kumar, 2005; Salcic, 2001).

FPGA-based system is a very flexible platform such that it can reduce development time greatly and benefit prototype research. As the complexity of hardware language VHDL (VHSIC hardware description language) design is growing fast, verification of design is complicated and exponential time consuming. This problem can be alleviated by FPGA, in which a modified design is implemented by simply downloading a bit stream file into FPGA and exercising the configured chip under its working environment (Kim, 2000). Many articles of FLCs have been published until now.

Salcic (2001) presented a generic fuzzy logic system of field-programmable logic device (FPLD) aimed at high-speed applications that could be easily customized for practical requirements. It implemented fuzzy logic systems that could vary in terms of number of inputs and outputs, their accuracy, membership functions, fuzzy rules, and speed.

Rani et al. (2005) described the hardware implementation of two-input/one-output fuzzy logic controller using VHDL. The architectural design was tested in Spartan FPGA chip. The maximum frequency of the clock and the total number of gates required for the hardware implementation of fuzzy logic controller were compared for the proportionally increasing number of rules.

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http://dx.doi.org/10.1016/j.eswa.2015.04.050
0957-4174/

Nomenclature

ADC	analog-to-digital conversion
A/D	analog to digital
ALMs	adaptive logic modules in ALTERA FPGA
ALTERA	FPGA company name
ALUTs	adaptive look-up tables in ALTERA FPGA
ASIC	application specific integrated circuit
AT2-FLC	type-2 average fuzzy logic controller
CAD	computer-aided design
COA	center of area method
COG	center-of-gravity
CPU	central processor unit
DC	direct current
DE	ratio of error
DUT	design under test
E	error signal
FAF	fuzzy accuracy factor
FBF's	fuzzy basis functions
FLC	fuzzy logic controller
FLIPS	fuzzy logic inferences per-second
FPGA	field programmable gate array
FPLD	field-programmable logic device
FRHC	fired rules hyper cube
FSM	finite state machine
FSR	full scale range
I/O	input/output
IT2-FIS	interval type-2 fuzzy systems
JTAG	joint test action group IEEE1149.1
K	10^3
LSB	least significant bit
LUT	look-up table
M	10^6
MF	membership function
MFG	membership function generator
MIMO	multi-input multi-output fuzzy system
MIN–MAX	fuzzy logic operation
MISO	multi-input single-output fuzzy systems
MODELSIM	mentor company simulation software name
MOM	mean of maximum method
Ms	millisecond
MSB	most significant bit
NB	negative big
NIOS II	altera company CPU's name
NM	negative median
NS	negative small
ns	nanosecond
O ()	time complexity
OC	output signal
PB	positive big
P&O	perturb and observe method
PI	proportional-integral
PM	positive median
PSO-GA	particle swarm optimization & genetic algorithm
PS	positive small
QUARTUS II	ALTERA company application software name
RAM	random-access memory
ROM	read-only memory
RTL	register transfer level
S	second
SOF	altera programmable bit stream file
SPEC	specification
SRT	square root
SSMF	shrinking span membership function
TCL	tool command language
TISO	two-input single-output
3-D	three-dimension
T1-FIS	type-1 fuzzy systems
μ_s	μ_s microsecond
VHDL	VHSIC hardware description language
ZO	zero

Srivastava, Kamalasadan, and Hande (2006) presented a comparative study of Shrinking Span Membership Function (SSMF) Fuzzy Logic Controller (FLC) relative to conventional FLCs. The fuzzy logic controller provided a means of converting a linguistic control strategy based on expert knowledge into an automatic control strategy. The SSMFs had different spans for various term set elements in the universe of discourse.

Three-dimensional fuzzy logic controller (3-D FLC) was developed for spatially-distributed parameter systems (Jiang, Zhang, Zou, & Cao, 2010). A table look-up scheme was employed to design 3-D FLC in terms of input-output pairs. A nearest neighborhood-clustering algorithm was employed to extract fuzzy rules from input–output data pairs, and then an optimization algorithm based on geometric similarity measure was used to reduce the obtained rule base (Zhang, Jiang, Zou, Qi, & Cao, 2011).

Maldonado and Castillo (2012) explained the design of a type-2 average fuzzy logic controller (AT2-FLC) on FPGA and its optimization using genetic algorithms. Type-1 fuzzy systems (T1-FIS) have exact membership functions (MF), while interval type-2 fuzzy systems (IT2-FIS) are described by membership functions with uncertainty. Interval type-2 fuzzy inference systems (IT2 FIS) can be used in applications of high speed processing. This is an important issue since the use of IT2 FIS still is controversial for several reasons. One of the most important is related to the shocking increase in computational complexity, even for small systems (Sepulveda, Montiela, Castillo, & Melin, 2012).

Analog implementation of Fuzzy Logic Controllers (FLCs) is an efficient method when speed, power, and area are critical (Pirbazari, Khoei, & Hadidi, 2013). Inference engine usually takes a large part of die area when the FLC has a large number of rules. For the fuzzier block, a new fully programmable IT2 membership function generator (MFG) circuit based on Type-1(T1) MFG is proposed that uses a new method for slope tuning (Mesri, Khoei, & Hadidi, 2013). The proposed slope tuning method, leads to smaller active area and significantly smaller total die area by reducing the numbers of required pins. Mokarram, Khoei, and Hadidi (2015) presented a CMOS FLC having the ability to support fractional polynomial membership functions.

Ramadan, El-Bardini, El-Rabaie, and Fkirin (2013) described an implementation of a fuzzy logic control (FLC) system and the conventional proportional-integral (PI) controller for speed control of DC motor, based on field programmable gate array (FPGA) circuit. A robust self-tuning scheme for fuzzy PI controllers was presented (De & Mudi, 2012). The output-scaling factor of the proposed controller is continuously adjusted by an updating factor that is defined on the normalized change of error of the controlled variable and the number of input linguistic variables.

Fired rules hyper cube (FRHC) based rule reduction technique was discussed and implemented on ADSP-BF537 processor (Maji, Patra, Mahapatra, Govindarajan, & Patel, 2013). A distributed fuzzy logic controller structure was designed for the single-link flexible manipulator (Shi, Zheng, Li, & Chen, 2012), whose structure would reduce the complexity of control systems. Gupta, Saini, and Saxena