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Practice Article

# Novel intelligent real-time position tracking system using FPGA and fuzzy logic

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ABSTRACT

The main aim of this paper is to test if FPGAs are able to achieve better position tracking performance than software-based soft real-time platforms. For comparison purposes, the same controller design was implemented in these architectures. A Multi-state Fuzzy Logic controller (FLC) was implemented both in a Xilinx® Virtex-II FPGA (XC2v1000) and in a soft real-time platform NI CompactRIO® –9002. The same sampling time was used. The comparative tests were conducted using a servo-pneumatic actuation system. Steady-state errors lower than 4 μm were reached for an arbitrary vertical positioning of a 6.2 kg mass when the controller was embedded into the FPGA platform. Performance gains up to 16 times in the steady-state error, up to 27 times in the overshoot and up to 19.5 times in the settling time were achieved by using the FPGA-based controller over the software-based FLC controller.



## 1. Introduction

### 1.1. Nature of the problem

In the scope of control practice, FPGAs are being used mainly to control electric motors, drives or converters. Only one reference was found about the hardware implementation of expert algorithms in a FPGA chip in order to control a servo-pneumatic system [1]. Relevant studies focusing on the comparison between the performance achieved by hardware-based and software-based real-time (RT) control architectures in servo-pneumatic actuation have not been reported. Only two preliminary studies were found about the performance gains with the use of FPGAs over Digital Signal Processors (DSP): one for single-phase PWM Inverter control [2] and another for real-time imaging processing [3]. Monmasson and Cirstea [4] reviewed the FPGA design methodologies already applied in industrial control problems, but they did not quantify the performance differences between the use of FPGAs and other platforms. The FPGA domain of use in relation with the software-based architectures is not clearly specified. Moreover, the optimization of the control performance is being conducted by splitting the control algorithm into an hardware part (HW) and a software part (SW) [5]. Without a clear understanding of the real potential of each control architecture performing complex control algorithms, it is not possible to design efficient hardware-software real-time implementation methods. Because the performance requirements for industrial control systems are increasing, knowledge on the performance achievements of such platforms is of utmost importance for industrial automation engineering and for research issues.

### 1.2. Background

FPGAs are hardware devices used as user-programmable Application Specific Integrated Circuits (ASICs). They are able to deal with complex engineering problems, being characterized for their: (a) parallel processing; (b) low cost, including the upgrade and implementation of redundancy methods; (c) high data throughput; (d) high reconfigurability; (e) high repeatability; (f) large bandwidth; (g) high flexibility; (h) open architecture; (i) low ratio design time/performance in relation with other control architectures; (j) high design portability; (k) platform independence; (l) easy integration; (m) high architecture efficiency; (n) broad commercial development and support; and (o) low power consumption [6]. The availability of software tools to generate efficient and flexible hardware description configurations automatically also brings easiness to the reconfiguration process. Moreover, FPGA designs can already be modeled, simulated and verified [7], as well as

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implemented with rapid prototyping tools [8]. They are being applied in many engineering scopes, such as in network processing, modulation systems, identification systems, monitoring systems, robotics, image analysis, speech recognition, simulation or power electronics. Expert algorithms are also being designed to run on FPGAs, such as the fuzzy logic, artificial neural networks, ant colony optimization, particle swarm optimization and prediction mechanisms.

Standard SW-based control platforms, such as DSPs and microprocessors, remain the top choice to carry out control operations. The development and configuration tools for SW-based systems are much more numerous than for FPGA-based systems, as well as the amount of available information and training courses. The major drawbacks of SW architectures in comparison with FPGAs have been: (a) longer sampling times; (b) higher cost, including the implementation of redundancy methods; (c) sequential processing of tasks; (d) higher probability of occurring systems faults; (e) more resources for RT execution of all required tasks, such as more complex memory resources and RT kernel architectures for task synchronization and scheduling; (f) difficulty to perform modifications in the hardware; and (g) lack of design portability [9]. These typical disadvantages of the SW-based architectures make them vulnerable to be replaced by low-cost and easily reconfigurable HW platforms.

FPGAs are reprogrammable devices suitable for the design of hard RT systems. They also highlight important advantages over standard SW-based hard RT systems. In relation with HW-based hard RT FPGAs, commercially available SW-based hard RT architectures: (a) are more expensive; (b) are more complex to program; (c) require longer design time; (d) have longer sampling time; (e) have not design portability; (f) need expert developers in the design of the RT architectures [10]. Open source SW-based hard RT architectures, such as the *RTLinux* for Linux kernels [10], are a readily available option. Expert designers are needed to carry out even few customizations and the design of an overall RT architecture becomes a quite hard and time consuming task, because the configuration of these kind of architectures is complex. FPGAs can also replace other types of ASICs due to their reconfigurability and shorter design time [11].

### 1.3. Outline

After this introductory section, Section 2 describes: (a) the experimental set-up; (b) the HW and SW platforms used in the experimental performance analysis; (c) the design methodology of the overall control system. Section 3 details the design and parameterization of the FPGA-based and SW-based control systems, as well as the control algorithms used to evaluate the position tracking performances. Experimental results and discussion are presented, respectively, in Sections 4 and 5. The main conclusions of the paper are reported in Section 6.

## 2. Material and methods

### 2.1. Experimental set-up

Fig. 1 shows the mechanical apparatus and the instrumentation of the servo-pneumatic machine. It is a one degree of freedom machine composed by:

- A double effect pneumatic cylinder (Festo CRDNGS 80-200-PPV-A), with a length of 200 mm and a diameter of 80 mm, which ensures 3016 N at 6 bar;
- A pneumatic servo-valve (Festo MPYE-5-1/8-HF-010-B), with a nominal flow rate of 700 l/min and 100 Hz of bandwidth, which controls the cylinder's spool position;

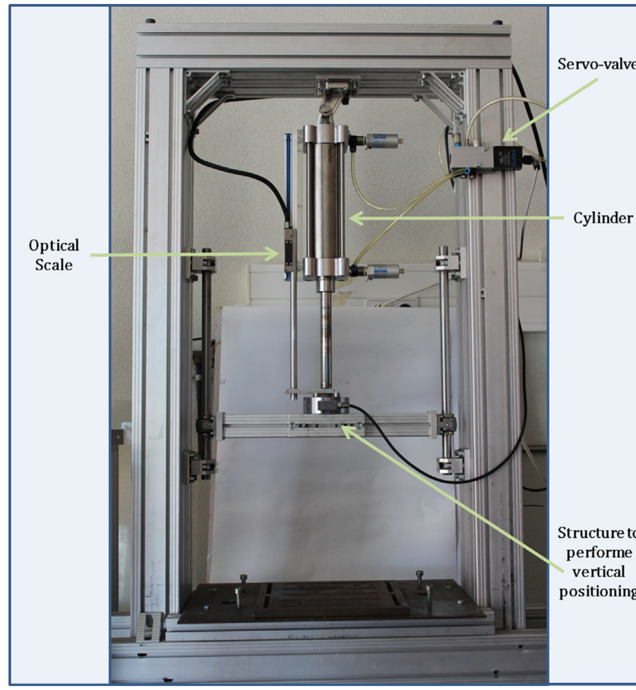


**Fig. 1.** Mechanical apparatus of the servo-pneumatic machine.

- An optical linear scale (Fagor SV-B220), with a resolution of 1 μm, which measures the cylinder's spool position.

### 2.2. Hardware and software platforms

This study was carried out with a National Instruments (NI) cRIO® platform, which is composed by: (1) a soft RT system NI cRIO-9002; (2) a reconfigurable chassis NI cRIO-9101, comprising a Xilinx® Virtex-II FPGA (XC2v1000); (3) a Digital Input NI cRIO-9411 and a 16 bit Analog Output NI cRIO-9263, which were used to perform Input/Output (I/O) operations.

#### 2.2.1. NI cRIO-9002

The NI cRIO-9002 features an industrial 195 MHz Pentium class processor to execute distributed and customizable real-time applications. Composed by 32 MB DRAM and 64 MB hard (storage) memories, programmatic communication over the network is possible using its 100 Mb/s Ethernet connection. With a 1 kHz clock and through a LabVIEW soft RT operating system (RTOS Phar Lap ETS 10.1), multithreaded embedded RT applications can be developed.

#### 2.2.2. NI cRIO-9101

The NI cRIO-9101 comprises a 40 MHz Xilinx® Virtex-II FPGA (XC2v1000) with one million gates, $40 \times 32$ arrays, 10240 LUTs and 720 Kbits of RAM to enable parallel, customizable and flexible hardware implementations. A local PCI bus connection provides data transfer rates up to 100 KB/s between the RIO FPGA and the soft RT processor. With LabVIEW 8.0, the cRIO-9101 platform ensures data transfer rates up to 2 KB/s through local networks.

#### 2.2.3. Development of the software platform

The overall control system software was implemented using LabVIEW 8.0 Professional Development System, LabVIEW Real-Time 8.0 and LabVIEW FPGA 8.0 modules.