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J China Univ Mining & Technol 2007, 17(1): 0068－0072

Design of Central Management & Control Unit for Onboard High-Speed Data Handling System

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Abstract: The Main Optical Telescope (MOT) is an important payload of the Space Solar Telescope (SST) with various instruments and observation modes. Its real-time data handling and management and control tasks are arduous. Based on the advanced techniques of foreign countries, an improved structure of onboard data handling systems feasible for SST, is proposed. This article concentrated on the development of a Central Management & Control Unit (MCU) based on FPGA and DSP. Through reconfigurating the FPGA and DSP programs, the prototype could perform different tasks. Thus the inheritability of the whole system is improved. The completed dual-channel prototype proves that the system meets all requirements of the MOT. Its high reliability and safety features also meet the requirements under harsh conditions such as mine detection.

Key words: space solar telescope; processing dataflow and control-flow separately; onboard data handling system; reconfiguration

CLC number: TP 332; V 4

1 Introduction

The Space Solar Telescope (SST) [1] is a scientific satellite observing the sun outside the earth atmosphere. The general objective is to achieve a breakthrough in solar physics by coordinated, wide spectral coverage, high resolution and continuous observations of transient and steady states in solar hydrodynamic and magnetic hydrodynamic processes.

As a major payload of the SST, the Main Optical Telescope (MOT) will determine vector magnetic and velocity fields in an imaging mode within 393–656 nm wave bands. There are different sampling rates of data and handling methods for different observation modes such as burst, active and quiet mode. For the eight 2048×1024 CCDs (Charge Coupled Devices) in the parallel channels of two-dimensional spectrograph (2DS) and a 2048×2048 CCD in the fast imaging channel, the sampling rate is up to 40 MB/s. Restricted by the satellite ground contact time, the quantity of downlink data is limited and we must carry on analyzing and processing real-time data in orbits such as image geometric rectification and radiation correction, silencing of noise, polarized parameter measurement and image compression [2]. In addition, the MOT has multiple working modes, many driver facilities and a precisely coordinated control is required especially for spectral selection, with a focus on dynamic adjustment of the correlation tracker system (CT) and the polarimeter for tight coupling. As well, management on these components will be very arduous. To ensure high-speed real-time data processing and reliability for control, we adopted a structure to process dataflows and control flows separately. A special scientific data processing unit was built under control of the MCU, which does not take part in data processing. It is preferred that the MCU manages all subunits for further coordination and for greater efficiency.

At present domestic onboard computers have largely adopted 8086/1753 which cannot meet the requirements of the SST. This paper introduces a re-

Received 04 June 2006; accepted 10 July 2006
Project 863-2.5.2.25 supported by the National High Technology Research & Development (863) Program of China
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configurable architecture based on the combination of FPGA and DSP, which delivers the very highest performance and a highly flexible signal process, required for the MOT. The paper also improves the inheritability of the system and saves development time and cost.

We first introduce the architecture of the onboard data handling system for the MOT and then focus on the design of the MCU, including the function, hardware and software, communication protocol and reliability design. At the end we provide the test results.

2 Architecture of the Onboard Data Handling System

With the development of large-scale satellites with more payloads and more tasks, the requirements for data handling and control are increasing. Fig. 1 shows the structure of the NEMO satellite [3]. This system considers the 48 Gbit state model mass memory as its core and the process dataflow and control flow are separated. The onboard image processor consists of 32 DSP processors in a parallel array. The characteristics of this system are a mass memory with a huge capacity and very complicated access control.

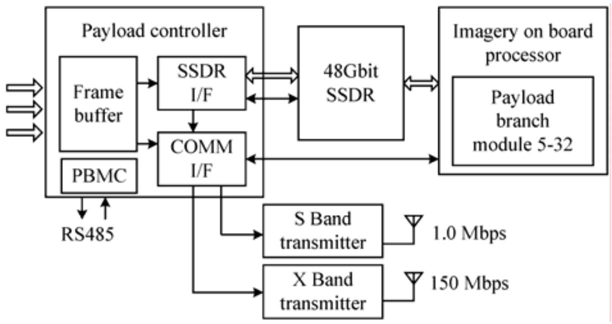


Fig. 1 Structure of NEMO

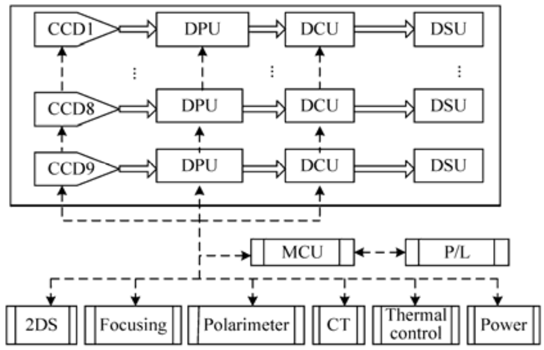
At present and in the near future, we cannot, as yet, develop a state-of-the-art model mass memory domestically, so we replaced the mass memory with Flash chips and assume the architecture to be suitable for the MOT, as shown in Fig. 2. This design makes it possible to develop the entire system domestically and improve the reliability of the parallel structure. The system has the following characteristics:

1) With a separate structure of processing dataflow and control flow, we solved the problems of real-time processing of huge amounts of data and a complex control.

2) Real-time processing data onboard will greatly reduce the requirements of memory and storage capacities or access complexity.

3) Every channel is parallel and independent, so the reliability is improved.

4) Management of payloads and control of data handling units will be done by the MCU in unison.



DPU: Data preprocessing unit; DCU: Data compressing unit; DSU: Data storage unit

Fig. 2 Structure of MOT

This article emphasizes the central management and control unit (MCU). The MCU does not take part in high-speed data processing and is mainly responsible for further coordination of all subunits to obtain higher efficiency. The housekeeping control and management on the MOT adopts a classified distribution structure. The dotted line and dual-line frame in Fig. 2 represents control layers and signals. The payload computer (P/L) is the first level, the MCU is the second and the control of all subunits is the third level. The system has an excellent arrangement and is highly reliable.

3 Function and Working Flow of MCU

As Fig. 3 shows, the work of the MCU can be divided into two stages: focusing and observing.

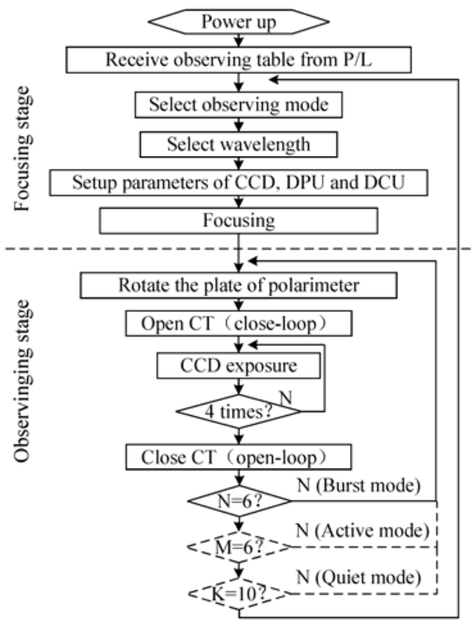


Fig. 3 Working flow of MCU

After being powered up, the MCU receives the observation table from the P/L, selects the work mode and waveband and then performs coarse and fine focusing recursively for 2DS, CT and the fast imaging channels. It then checks the current, voltage and