INTEGRATION, the VLSI journal 43 (2010) 136–155

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

Analog circuits optimization based on evolutionary computation techniques

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ARTICLE INFO

Article history:
Received 22 December 2008
Received in revised form
1 June 2009
Accepted 12 September 2009

Keywords:
Design automation
Analog integrated circuit synthesis
Evolutionary optimization
Learning strategies

ABSTRACT

This paper presents a new design automation tool, based on a modified genetic algorithm kernel, in order to improve efficiency on the analog IC design cycle. The proposed approach combines a robust optimization with corner analysis, machine learning techniques and distributed processing capability able to deal with multi-objective and constrained optimization problems. The resulting optimization tool and the improvement in design productivity is demonstrated for the design of CMOS operational amplifiers.

1. Introduction

The microelectronics market, with special emphasis to the production of complex mixed-signal systems-on-chip (SoC), is driven by three main dynamics, time-to-market, productivity and managing complexity [1]. Pushed by the progress in nanometer technology, the design teams are facing a curve of complexity that grows exponentially, thereby slowing down the productivity design rate. Analog design automation tools are not developing at the same pace of technology, once custom design, characterized by decisions taken at each step of the analog design flow, relies most of the time on designer knowledge and expertise. Actually, the use of design management platforms, like the Cadence® Virtuoso platform, with a set of integrated CAD tools and database facilities to deal with the design transformations from the system level to the physical implementation, can significantly speed-up the design process and enhance the productivity of analog/mixed-signal integrated circuit (IC) design teams. These design management platforms are a valuable help in analog IC design but they are still far behind the development stage of design automation tools already available for digital design [2–4]. Therefore, the development of new CAD tools and design methodologies for analog and mixed-signal ICs is essential to increase the designer's productivity and reduce design productivity gap.

The work presented in this paper describes a new design automation approach to the problem of sizing analog ICs. ;The developed design optimization tool, GENOM, is based on a modified genetic algorithm (GA) kernel and incorporates heuristic knowledge on the control mechanism allowing a significant reduction on the required number of generations and, therefore, iterations to reach the optimal solution. However, the optimization process, employing a simulation-based approach with a kernel based on stochastic optimization techniques is clearly a computational intensive task typified by high dimension search spaces and high cost function evaluations. A step forward to enhance the efficiency of the implemented optimization tool corresponds to the introduction of behavior modeling techniques. The model introduced in this paper follows a supervised learning strategy based on support vector machines (SVM) [11,64] which, together with an evolutionary strategy, is used to create feasibility models in order to efficiently prun the design search space during the optimization process, thus, reducing the overall number of required evaluations [12,13].

The paper is organized as follows: Section 2, presents a state-of-the-art overview for analog IC design automation; Section 3, describes the architecture of the proposed design automation environment GENOM; Section 4, discusses the proposed optimization kernel based on evolutionary computation methods. Section 5, describes the kernel enhancements with design knowledge automatically generated using well-known learning strategies. Then, in Section 6, the proposed approach is demonstrated for the design of CMOS operational amplifiers. Finally, the conclusions are drawn in Section 7.

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doi:10.1016/j.vlsi.2009.09.001

2. State-of-the-art: overview

2.1. Automated circuit synthesis approaches

A typical design flow for analog and mixed-signal IC circuits (AMS) consists of a series of design steps from the system level to the device level [14–16]. The steps between any two of these hierarchical levels involve topology selection, circuit sizing and design verification.

The sizing task receives a topology description, a set of performance specs and a technology reference and produces a sizing solution for each block depending on the abstraction level. Several solutions were proposed derived from either knowledge-based methods or optimization-based approaches as depicted in Fig. 1.

The knowledge-based approach presented, in programs like BLADES [17], IDAC [18], OASYS [19], MDAC/ALSC [20,21] and [41-45], was the first to appear and is characterized by including a complete design plan, describing how the circuit components must be sized to reach the optimum solution of the design problem. For example, the IDAC tool [18] takes advantage of the designer experience to manually derive or rearrange design plans, while, OASYS [19] is built over a library of design plans defined for each elementary building block of the library, allowing the representation of hierarchical topologies defined as the interconnection of several elementary building blocks.

The optimization-based approach uses an optimization engine, instead of a design plan, to perform the design task. The optimization process is an iterative procedure where design variables are updated at each iteration until they achieve an equilibrium point. Concerning performance evaluation, the evaluation engine is typically implemented using an equation-based optimization, a simulation-based optimization or a behavioral-based optimization approach.

The equation-based methods use analytic design equations to evaluate the circuit performance. These equations can be derived manually or automatically by symbolic analysis tools. Then, the problem can be formulated as an optimization problem and normally solved using a numerical algorithm. Some of the most relevant approaches are OPASYN [22], STAIC [23], MAULIK [24], ASTRX/OBLX [25], AMGIE [7], GPCAD [8,26], SD-OPT [27], TAGUS [9,10] and [35,36]. A promising methodology that has received much attention is related to circuit problems formulated in posynomial form and seen in tools like GPCAD. These techniques take advantage of the development of extremely powerful and efficient interior-point methods for general convex optimization problems [27].

The simulation-based approaches, such as, FRIDGE [28], DELIGHT.SPICE [5], FASY [29], ANACONDA [6], MAELSTROM [30], DARWIN [31] and [37-40], consist of using some form of simulation to evaluate the circuit's performance. In general, these types of tools employ a circuit analysis tool in the inner loop of the optimization cycle to determine the circuit's performance.

A step forward to enhance the efficiency of optimization-based methods is introduced by a new class of modeling techniques based in learning strategies. In this class of methods, the behavior of the circuit to be optimized is modeled by a learning mechanism based on the distribution of variation parameters, thus allowing a quick evaluation of the performance for a specific set of design parameters. Some of the most significant behavioral-based methodologies are described by Alpaydin et al. [32], Vincentelli [33] and Vemuri [34].

Besides these efforts some commercial EDA tools for circuit sizing have emerged in the past few years, such as the ADA's [48] Genius product line now integrated in Synopsis, Barcelona Design [8] which employ convex optimization techniques and recently the NeoCircuit from Neolinear Inc. [47], which implements a simulation-based approach.

2.2. Design automation tools: comparative analysis

The existing design automation approaches are here compared, taking into account both qualitative and qualitative measures.

The computation time is highly correlated with the nature of the evaluation engine. In the knowledge-based approaches the execution speed is the highest of all methods, considering that,

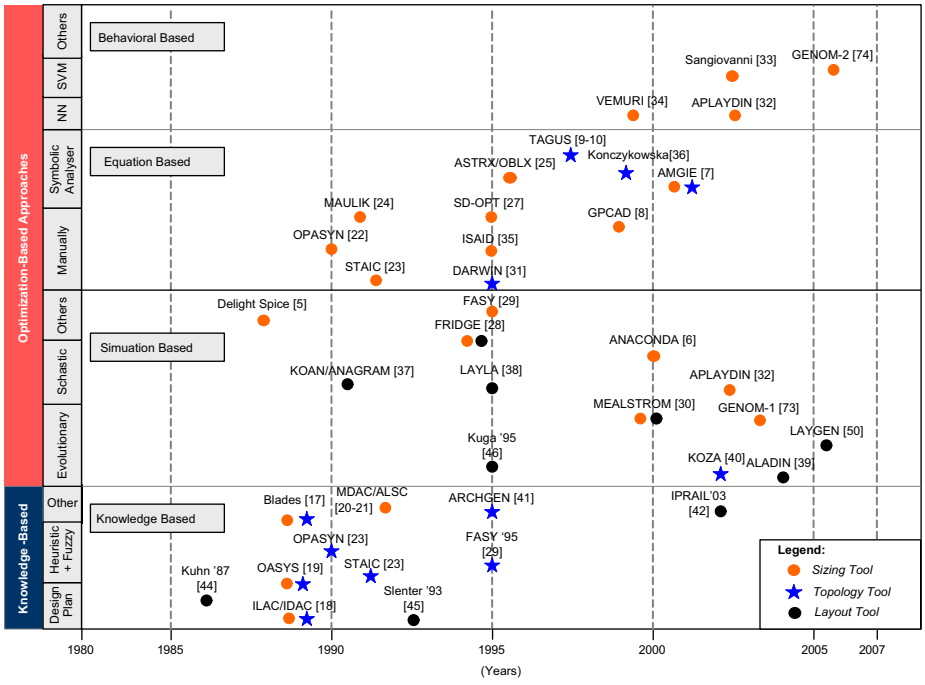

Fig. 1. Overview of analog IC design automation tools (upgrade from [3]).