Electric Power Systems Research 81 (2011) 967–973

Contents lists available at ScienceDirect

Electric Power Systems Research

journal homepage: www.elsevier.com/locate/epsr

A proposal for standard VSC HVDC dynamic models in power system stability studies

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ARTICLE INFO

Article history:
Received 4 January 2010
Received in revised form 24 October 2010
Accepted 30 November 2010
Available online 3 January 2011

HVDC converters
HVDC transmission
HVDC transmission control
Power system modelling
Power system simulation

ABSTRACT

In this paper, two standard VSC HVDC dynamic models are proposed. The full system model, consisting of the converter and its controllers, DC circuit equations, and coupling equations, is derived mathematically. Special attention is given to the filter and phase-locked loop (PLL), often neglected in VSC HVC modelling. A reduced order model is then derived from the full model by neglecting the smallest time constants, resulting in a reduced set of differential equations that can be integrated with a larger time step. The models are implemented in *MatDyn*, a Matlab based stability program. Simulations validate the proposed models.

1. Introduction

Power system stability studies require phasor models of the various equipments present in the modern power system, such as generators and their controls, FACTS devices, and loads. In most power system software, the user can select models from a standard models library or specify his own, user-defined models. Using standard models for power system equipment has certain advantages. Data exchange between utilities, and the transition to new software packages proves much more convenient if standard models are used. Furthermore, standard models can be used for a wide range of studies. In the planning stage, when the details of the equipment are not yet known, standard models can be used. In order to obtain acceptable results, the generic models should be quite detailed. We call such models 'full models'. If the equipment is located far away from the part of the system under study, the equipment can be modelled with less detail; we refer to such models as 'reduced' models. Only for a detailed study of a part of the system where the equipment plays a prominent role, standard models should not be used. A model that very closely mimics the behaviour of the actual system is needed. Such a 'detailed model' is usually delivered by the manufacturer. An example of this approach are stability studies in the early days of computer simulation of power systems when it was common practice to represent all generators by the classic generator model, and only a few generators of interest by detailed models of the generators and their controls.

Standard models exist for numerous power system equipment, such as excitation systems [1], and steam and hydro turbines [2]. However, to the authors' best knowledge, no standard models for VSC HVDC have been proposed in literature. We believe there is a need for generic, standard models for VSC HVDC systems. VSC HVDC has an increasingly wide range of application in the power system [3]. Hence, it is clearly an area of interest and receives a lot of attention. Quite some research papers are dedicated to the subject of modelling VSC HVDC systems [4–7]. However, most of these models are not generic, e.g. the model in [6] is derived explicitly for twelve pulse converters [4,7] are only valid for systems using Pulse Width Modulation (PWM).

This paper proposes two standard VSC HVDC dynamic models for power system stability studies, that are generic, i.e. valid regardless of power electronics topologies. The phasor modelling approach is used in this paper, as is customary in transient stability studies. First, a full model will be constructed: the converter equations, equations of the DC circuit and coupling equations are derived in Section 2. In Section 3, the controller equations are appended to the system of equations to get the complete system of equations for the full model. Next, a reduced order model is derived in a mathematically rigorous way in Section 4. Lastly, simulations validate and compare the proposed models (Section 5).

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doi:10.1016/j.epsr.2010.11.032

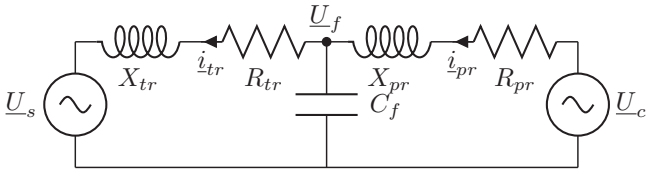

Fig. 1. One-line diagram of the AC Circuit with filter. $\underline{U}_s$ is the system voltage, $\underline{U}_c$ the converter voltage.

2. VSC HVDC model

2.1. Converter

VSC HVDC converters are connected to the system through a phase reactor and a transformer. A filter is connected between the phase reactor and the transformer (Fig. 1). It was shown in [8], that the filter behaves as a pure capacitor at system frequency. The basic equations of this circuit,

$$u_c - u_f = L_{pr}\frac{di_{pr}}{dt} + R_{pr}i_{pr}, \tag{1}$$

$$u_f - u_s = L_{tr}\frac{di_{tr}}{dt} + R_{tr}i_{tr}, \tag{2}$$

$$i_{pr} = i_{tr} + C_f\frac{du_f}{dt}, \tag{3}$$

are transformed to a rotating reference frame:

$$\frac{di_{pr}^d}{dt} = -\frac{R_{pr}}{L_{pr}}i_{pr}^d + \omega i_{pr}^q + \frac{1}{L_{pr}}(u_c^d - u_f^d), \tag{4a}$$

$$\frac{di_{pr}^q}{dt} = -\frac{R_{pr}}{L_{pr}}i_{pr}^q - \omega i_{pr}^d + \frac{1}{L_{pr}}(u_c^q - u_f^q), \tag{4b}$$

$$\frac{di_{tr}^d}{dt} = -\frac{R_{tr}}{L_{tr}}i_{tr}^d + \omega i_{tr}^q + \frac{1}{L_{tr}}(u_f^d - u_s^d), \tag{5a}$$

$$\frac{di_{tr}^q}{dt} = -\frac{R_{tr}}{L_{tr}}i_{tr}^q - \omega i_{tr}^d + \frac{1}{L_{tr}}(u_f^q - u_s^q), \tag{5b}$$

$$\frac{du_f^d}{dt} = -\omega u_f^d + \frac{1}{C_f}(i_{pr}^d - i_{tr}^d), \tag{6a}$$

$$\frac{du_f^q}{dt} = \omega u_f^q + \frac{1}{C_f}(i_{pr}^q - i_{tr}^q). \tag{6b}$$

The angle ωt is provided by the phase-locked loop (PLL), arbitrarily assumed here to align system voltage with the q-axis.

2.2. Phase-locked loop

In general, a PLL is "a circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal in frequency as well as in phase." [9, p. 1]. It is a control system that acts on the phase difference between the reference signal and the output, such that the phase of the output is locked to the phase of the reference [9, p. 1]. All PLLs consist of three basic components: a phase detector (PD), a voltage controlled oscillator (VCO), and a loop filter (LF). The phase detector compares the phase of the input or reference signal with the phase of the output signal, produced by the voltage controlled oscillator. The voltage controlled oscillator produces an oscillating signal with a frequency determined by the output signal of the loop filter. The loop filter removes noise and high frequency signals, and is responsible for the control of the PLL. Here the circuit of Fig. 2 is used. It is a type 2 loop, most prevalent

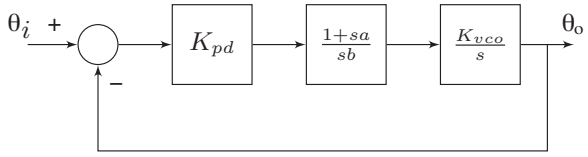

Fig. 2. PLL implementation.

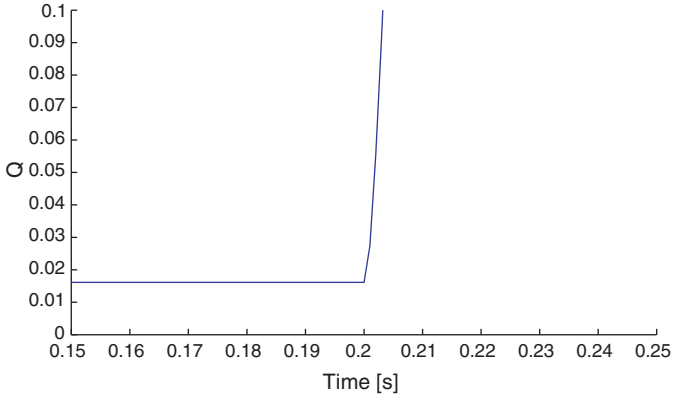

Fig. 3. Converter reactive power without PLL (close up).

in phase-locked loops [10, p. 16]. The differential equations of the system are:

$$\dot{x} = bK_{pd}(\theta_i - \theta_o), \tag{7}$$

$$\dot{\theta_o} = K_{vco}(bK_{pd}(\theta_i - \theta_o) + ax). \tag{8}$$

The design of the PLL can have a large influence on the dynamic behaviour of the system. Therefore, it is now common practice to include a detailed PLL model in electromagnetic programs. A problem that can occur is that during or immediately after abnormal system conditions such as faults, the PLL is not able to lock, and consequently does not produce a correct phase signal. Another problem is the operation in weak AC grids: the angle settling time after disturbances is slow, while the current loop is fast. To correctly study this kind of behaviour and interactions, a phasor model is not sufficient, as it can not capture the behaviour of the PLL in abnormal system conditions and weak AC grids. A detailed electromagnetic model needs to be used. In phasor models it is therefore less common to include the PLL. However, it has been shown in some contributions that the PLL has an influence on stability. A PLL introduces a small delay which is here in the order of 1 ms. In [11], it has been shown that the PLL delay can cause undesired power exchange. To investigate the influence of the PLL on power system stability, we perform simulations with and without PLL, using modified versions of MATPOWER [12] and *MatDyn* [13]. At $t = 0.2$, a large load with P and Q component is switched in. Fig. 3 shows a close up around $t = 0.2$ of the converter's reactive power output when no PLL is included in the model. If a PLL is modelled, its time delay causes the reactive power output to drop first (Fig. 4), in accordance with the results obtained in [11]. When looking at overal reactive power output (Figs. 5 and 6), it can be seen that the difference is very small and does not significantly impact the other state variables, and thus can be safely neglected in power system stability studies.

2.3. Filter

Many models proposed in literature do not take into account the filter bus, e.g.: [4–6,14]. The one-line diagram is then simplified