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Future of nano CMOS technology

Hiroshi Iwai

Frontier Research Center, Tokyo Institute of Technology, Yokohama, Japan

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ABSTRACT

Although Si MOS devices have dominated the integrated circuit applications over the four decades, it has been anticipated that the development of CMOS would reach its limits after the next decade because of the difficulties in the technologies for further downscaling and also because of some fundamental limits of MOSFETs. However, there have been no promising candidates yet, which can replace Si MOSFETs with better performance with low cost. Thus, for the moment, it seems that we have to stick to the Si MOSFET devices until their end.

The downsizing is limited by the increase of off-leakage current between source and drain. In order to suppress the off-leakage current, multi-gate structures (FinFET, Tri-gate, and Si-nanowire MOSFETs) are replacing conventional planar MOSFETs, and continuous innovation of high-k/metal gate technologies has enabled EOT scaling down to 0.9 nm in production.

However, it was found that the multi-gate structures have a future big problem of significant conduction reduction with decrease in fin width. Also it is not easy to further decrease EOT because of the mobility and reliability degradation. Furthermore, the development of EUV (Extremely Ultra-Violet) lithography, which is supposed to be essential for sub-10 nm lithography, delays significantly because of insufficient illumination intensity for production. Thus, it is now expected that the reduction rate of the gate length, which has a strong influence on the off-leakage current, will become slower in near future.

1. Introduction

Large Scale Integrated circuits (LSIs), which started in early 1970s as memories [1] and microprocessors [2] using 10 μm p-channel MOSFETs, have evolved to 14 nm CMOS VLSIs (Very large Scale Integrated circuits) as shown in Fig. 1. During the past 44 years, we have experienced 19 generations for the downsizing, contributing to the continuation of the Moore's law [3]. Every 2.5 years in average, the line width and area for a MOSFET decreases with factor of 0.7 and 0.5, respectively. As the result, the line width and area reduced by 500 and 250,000 times in 44 years, and the fabrication cost per single MOSFET decreased tremendously. Not only the number of the MOSFETs in a single LSI chip increased, but also the performance – such as operational speed and power consumption per computational operation or function – of LSIs was enhanced dramatically because of decrease in capacitance and supply voltage. Just for example, today's largest capacity SD (Secure Digital) memory card stores 256 GB (Bite) or 2 Tbit information. However, its volume is only $2.4 \times 3.2 \times 0.2\ cm^3$, its weight is 2 g, its supply voltage is 3 V, and the maximum power consumption is about 1 W, i.e. only 0.5 pW per bit.

Now, entering the smart society, the amount of the information and data treated by semiconductor devices keeps growing explosively. Corresponding to the growth, the market for integrated circuits are expected to increase 5 times in next 10 years [4] and demands for the low power, high-performance LSIs becomes stronger and stronger. LSIs are matured products with the history of already more than 40 years, started in early 1970s. It is tremendous that the market of such matured products still keeps growing with the high rate.

Corresponding with increase in the market, the energy consumed by the operation of LSIs reached the level which cannot be ignored among the global energy consumption, and thus, the suppression of the power consumption of the LSIs becomes very important. Basically, the decrease in the power consumption can be accomplished by the reduction of the capacitance of the device and supply voltage used for the devices, and thus, the continuation of the downsizing is critically important. At the beginning of the last century, electronics started with the invention of vacuum tube as the 1st generation of electron devices. At that time, the typical size of the vacuum tube was about $5 \times 5 \times 10\ cm^3$, its weight was about 100 g, supply voltage was 220–100 V, and the maximum power consumption is about several tens W. If we assume to realize a 1 Tbit (or 128 GB) memory using that vacuum tubes, the size,

E-mail address: iwai.h.aa@m.titech.ac.jp

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0038-1101/

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm→ 0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm → 90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm(2012) → 14 nm (2014)

Fig. 1. Trend of downsizing for MOS integrated circuits.

weight, and power consumption would be anomalously huge as $0.5 \times 0.5 \times 1\ km^3$,100 M ton, and 50 TW (assuming 50 W per vacuum tube), respectively. The size is much bigger than the world tallest building, the weight is more than 100 times heavier than the world heaviest ship, and the power consumption corresponds to the power generation of 50,000 nuclear reactors. By comparing with the SD card case described before, the effect of the downsizing on power consumption by the development of micro and nano technology is very significant. In this paper, current status of nano-CMOS technology is reviewed and future of nano-CMOS technology is discussed.

2. Downsizing limit

Logic CMOS LSI technology reached that of 90 nm node about 10 years ago, and nano CMOS era started. What was the specific for nano CMOS, differing from micro CMOS? In early 1990s, it had been dreamed that nano-electronics would bring us something new fancy effects due to its small size, e.g. quantum mechanical effects. However, as long as in the logic CMOS devices are concerned, nothing especially new fancy thing had happened, and most of the change from micro to nano was almost predictable conventional type change due to the geometry reduction.

Also, in the logic device world, no other nano-electronic devices than CMOS had emerged which can really replace CMOS. Thus, the most important question for the logic devices today would be "What will limit the downsizing of MOSFET?" Several causes, such as lithography limit, resistance and capacitance increase of interconnects, or huge cost of production would be considered as the answer. Although the variability of the MOSFET characteristics is a big concern, the biggest problems of the variability are those for the threshold voltage and subthreshold slope which are directly connected to off-leakage current variation. Thus, the most critical cause to limit the downsizing is the off-current increase for the MOSFETs.

There are basically four types of the off-leakage current components, (a) punch-through (drain bias induced or short channel induced), (b) subthreshold (source electron energy distribution induced), (c) direct-tunneling between source and drain, and (d) gate oxide leakage current; all of which are becoming critical issues for the downsizing.

2.1. Punch-through off-leakage current

When decreasing the channel length of the MOSFETs, space charge region or depletion region created by the drain bias touches to the source as shown in Fig. 2. Because the potential of the depletion layer is positive (n-MOSFET case just for example), electrons in the source flow into the deletion region and then, reach the drain even when applying 0 V to the gate electrode in order to make the MOSFET off. Thus, off-leakage current will limit the downsizing.

In order to decrease the depletion layer width, drain voltage or supply voltage of the MOSFETs should be decreased with the downsizing as shown in Fig. 2. This has been done in the past, but the pace of the supply voltage reduction has been very slow recently because of the difficulty in decreasing the threshold

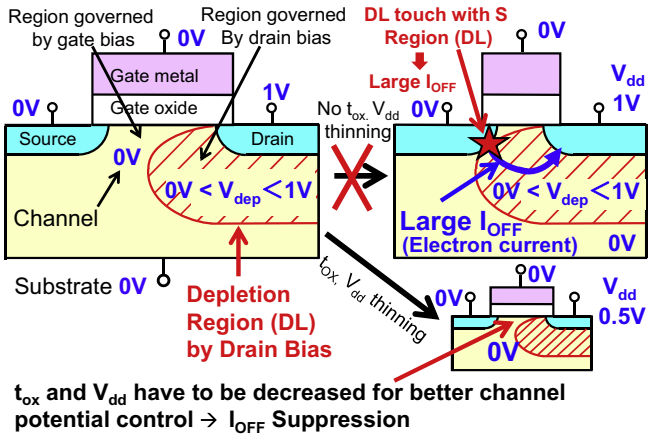

Fig. 2. Relation between the depletion layer and 'punch-through' off-leakage current.

voltage. The threshold voltage reduction increases subthreshold leakage current as explained later.

Another method to decrease the depletion layer width is thinning the gate oxide thickness in order to increase the electric field between the gate electrode and channel, so as to enhance the gate bias controllability of the channel potential as shown in Fig. 2. By thinning the gate oxide thickness, channel potential is more influenced by gate bias than by drain bias. This has been done also in the scaling scheme [5] for many years until now. We do need to continue the gate oxide thinning. However, thinning the EOT (Equivalent oxide thickness) is very difficult as explained later.

The third method is to make the entire Si channel layer thin. The potential of the channel region just underneath the gate electrode is easy to be controlled by the gate bias. This is the concept of Fully Depleted (FB), Ultra-Thin Body (UTB) or Extremely Thin (ET) SOI [6] as shown in Fig. 3 (see Fig. 4).

The fourth method is to provide another gate electrode at the bottom of the thin Si channel to enhance the controllability of

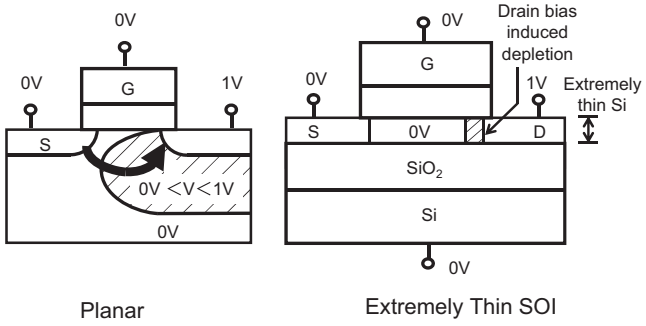

Fig. 3. Planar and extremely thin SOI MOSFETs.

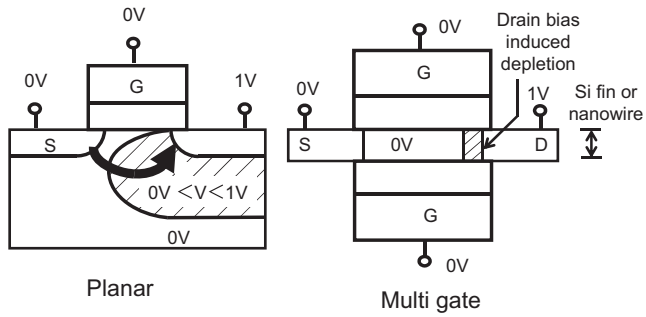

Fig. 4. Planar and multi gate MOSFETs.