A New Algorithm for the Generation of Reference Voltages of a DVR Using the Method of Instantaneous Symmetrical Components

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Abstract: This letter presents a new method for the generation of reference voltage for a dynamic voltage restorer (DVR). These voltages, when injected in series with a distribution feeder by a voltage source inverter, can tightly regulate the voltage at the load terminal against imbalance or harmonics in the source side. It is stipulated that the DVR does not supply any real power in the steady state. The reference voltage generation scheme is validated through digital computer simulation studies.

Keywords: Dynamic voltage restorer, series compensation.

Introduction: A power electronic converter-based series compensator that can protect critical loads from supply side voltage disturbances other than outages is called a dynamic voltage restorer (DVR). It injects a set of three-phase ac output voltages in series with the distribution feeder voltages. The amplitude and phase angle of the injected voltages are variable, thereby allowing control of the real and reactive power exchange between the DVR and the distribution system. This letter extends the concept of dynamic voltage restoration further to discuss a DVR that can tightly regulate the load voltage without any real power consumption in the steady state. It can also perform the primary functions of the restorer—i.e., to protect the load from temporary voltage interruption, sag/swell, etc. In particular, the reference voltage generation scheme for the DVR is discussed. These voltages, when injected in series with the system via an inverter, perform the desired task of voltage regulation. The voltage generation scheme is validated through extensive simulation studies.

Expression for Real Power in Terms of Instantaneous Symmetrical Components: In this section we define the real power in terms of instantaneous symmetrical components. These components are defined for three instantaneous currents i_a, i_b, and i_c as [1]

$$i_{a012} = \begin{bmatrix} i_{a0} \\ i_{a1} \\ i_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{1}$$

where $a = e^{j120^\circ}$ and zero, positive, and negative sequence currents are denoted by subscripts 0, 1, and 2, respectively. It is to be noted that i_{a0} is zero for balanced currents and the phasor i_{a2} is the complex conjugate of the phasor i_{a1}. A similar transformation can also be defined for voltages.

The instantaneous power in a three-phase system is defined as

$$p = v_a i_a + v_b i_b + v_c i_c. \tag{2}$$

Substituting the inverse transform from (1) into (2) we get

$$p = v_{a0} i_{a0} + v_{a1} i_{a2} + v_{a2} i_{a1} = v_{a0} i_{a0} + v_{a1} i_{a1}^* + v_{a1}^* i_{a1} = v_{a0} i_{a0} + 2\mathrm{Re}\left(v_{a1} i_{a1}^*\right). \tag{3}$$

Reference Voltage Generation for DVR: The proposed voltage regulation scheme is shown in Figure 1. This consists of the following:

- DVR: represented by voltage sources v_{fa}, v_{fb}, and v_{fc};
- Supply voltage: represented by sources v_{sa}, v_{sb}, and v_{sc}.

The DVR is connected between a terminal bus on the left and a load bus on the right. The voltage sources are connected to the DVR terminals by a feeder with an impedance $R + jX$. We shall assume that the loads are balanced and the load impedance is given by $Z_l = R_l + jX_l$. The incoming bus of the DVR is referred to as the terminal bus while the outgoing bus is referred to as the load bus with their respective quantities being denoted by subscripts t and l, respectively.

It is convenient that the DVR reference voltages are generated based on the measurement of the local variables only. In addition, we stipulate that the DVR does not supply (or consume) any real power in the steady state. Since the desired load voltages are balanced sinusoids and the load is balanced, the instantaneous load power is constant and this must be equal to the average power entering the DVR terminal bus. Thus from (3) we get

$$p_l = 2\mathrm{Re}\left(v_{la1} i_{sa1}^*\right) = 2|v_{la1}||i_{sa1}|\cos\left(\theta_{vla1} - \theta_{isa1}\right) = p_{tav} \tag{4}$$

where θ_{vla1} and θ_{isa1} are the angles of the vectors v_{la1} and i_{sa1}, respectively, and p_{tav} is the average power entering the terminal bus. From (4) we get

$$\theta_{vla1} = \cos^{-1}\left(\frac{p_{tav}}{2|v_{la1}||i_{sa1}|}\right) + \theta_{isa1}. \tag{5}$$

We now define the desired instantaneous symmetrical components of the load voltage as

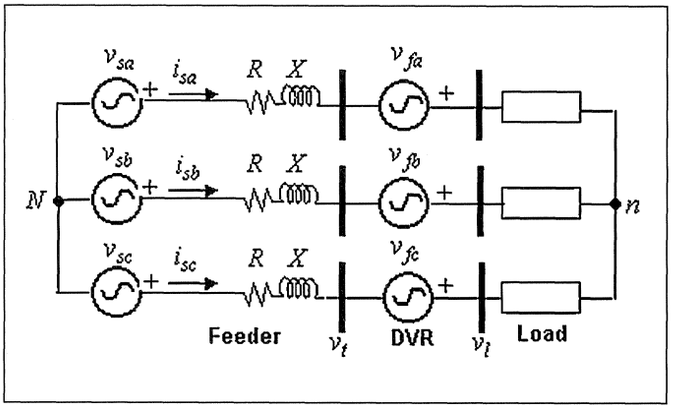

Figure 1. Schematic diagram of a DVR connected power system

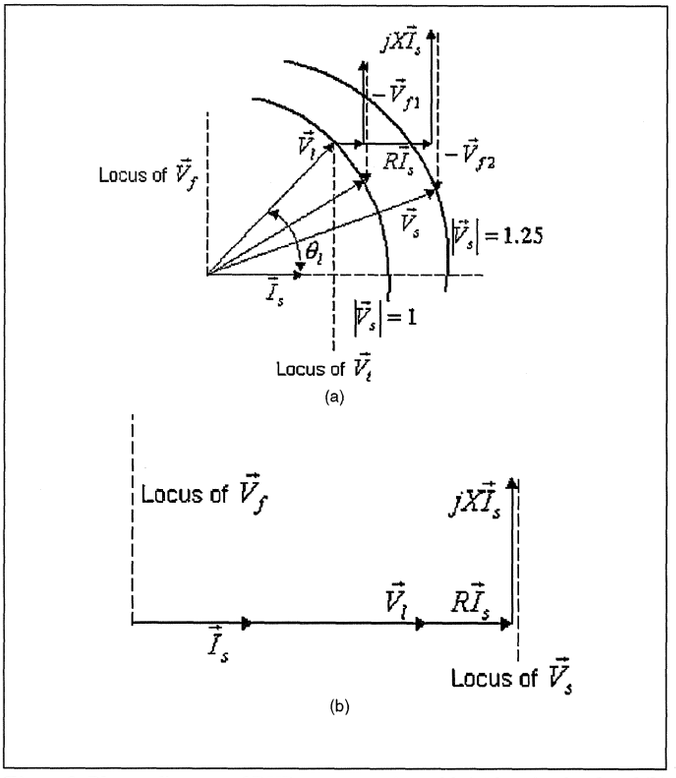

Figure 2. Phasor diagram of DVR compensation with (a) lagging load and (b) resistive load

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$$\begin{bmatrix} v_{la\,0} \\ v_{la\,1} \\ v_{la\,2} \end{bmatrix} = \sqrt{\frac{3}{2}} \begin{bmatrix} 0 \\ V_{l\text{rms}} e^{j\theta_{vla\,1}} \\ V_{l\text{rms}} e^{-j\theta_{vla\,1}} \end{bmatrix} \quad (6)$$

where $V_{l\text{rms}}$ is the desired rms value of the load voltage. Then the instantaneous load voltages are generated from (6) by the inverse of transform given in (1). Once the instantaneous load voltages are obtained, the reference filter voltages are obtained from the relation (see Figure 1)

$$v_{fk}^{*} = v_{lk} - v_{tk}, \quad k = a, b, c. \quad (7)$$

Load Voltage Regulation Using DVR: The phasor diagram of the compensated system in the steady state is shown in Figure 2. Since the DVR must not inject any real power, the DVR voltage must be in quadrature with the line current $\vec{I}_s$. Figure 2(a) shows the operation with a load current having lagging power factor. It is to be noted that the power factor angle θ_l is dependent on the load and is independent of the feeder impedance. In this figure it is assumed that the rms load voltage is to be regulated at 1.0 per unit. The figure shows two operating points—one with source voltage of 1.0 per unit and the other with 1.25 per unit. This implies that with the system operating with a source voltage of 1.0 per unit, sudden swell in this voltage to 1.25 per unit can be compensated by changing the injected voltage from $\vec{V}_{f1}$ to $\vec{V}_{f2}$. Similarly, a voltage sag can also be compensated up to a certain drop in the source voltage. It is to be noted that for a constant $|\vec{V}_s|$, if the load current increases, the phasor for $\vec{V}_s$ moves clockwise along a circular arc. The limit of compensation is reached when $\vec{V}_s$ is in phase with $\vec{I}_s$. It is interesting to note that if the feeder resistance R in Figure 1 is negligible, $\vec{V}_s$ and $\vec{V}_l$ coincide and the DVR compensates for the entire feeder drop.

Figure 2 (b) shows the operation with a purely resistive load. It can be seen that it is impossible to regulate with equal $|\vec{V}_s|$ and $|\vec{V}_l|$. The maximum value of $|\vec{V}_l| / |\vec{V}_s|$ can be achieved when $\vec{V}_s$ is in phase with $\vec{I}_s$, i.e., the DVR compensates for the entire feeder reactive drop.

Example 1: In this example we shall assume that both load and source are balanced and the DVR is required to regulate the load voltage. It is assumed that the DVR is ideal and has perfect tracking, i.e., $v_f = v_f^{*}$. We have used a three-phase, four-wire distribution system, even though the formulation is also valid for a three-wire system. The system parameters chosen for the study are: feeder impedance = 0.05 + j0.3 per unit, load impedance = 2.5 + j2 per unit, system frequency = 50 Hz, and source voltage (rms) = 1.0 per unit.

The system response when the DVR reference voltages are produced by (7) is shown in Figure 3. Note that in this and all subsequent figures that display three phase quantities, the phases a, b, and c are plotted using solid, dashed, and dotted lines, respectively. The power average (p_{tav}) is obtained by a moving average (MA) filter. The DVR is connected at the end of first half cycle after p_{tav} is obtained. It can be seen from Figure 3(a) that the load voltages have a peak value of $\sqrt{2}$ per unit. However, the line currents are not balanced and the DVR voltage is distorted, as evident from Figures 3(b) and (c), respectively. The DVR power is oscillating, even though the mean of the oscillation is zero as stipulated by (4). The reason for this unusual behavior is that the sudden connection of the DVR at the end of the first half-cycle temporarily unbalances the line current. This causes a transient violation of (4) as p_{tav} is not equal to $2|v_{la\,1}||i_{sa\,1}|\cos(\theta_{vla\,1} - \theta_{isa\,1})$ as the line currents are no longer balanced. Without any corrective mechanism, the DVR cannot be forced to correct for this violation. This leads to a steady state with distortion in its voltages.

Extraction of Fundamental Positive Sequence: To avoid the above-mentioned problem we note that the DVR must inject voltage in such a way that the load voltage contains fundamental positive sequence only. As the load is balanced, the load currents will also contain fundamental positive sequence only. The real power at the load terminal then depends only on the positive sequence of load voltage and load (line) current as required by (4). Thus, at the instant of connection of the DVR, the fundamental of positive sequence of the line current must be used in (4). Therefore, we need to extract the fundamental of positive sequence of the phasor load current, denoted by $i_{sa\,1\_f}$. This can be directly computed from the instantaneous samples of $i_{sa\,1}$ as

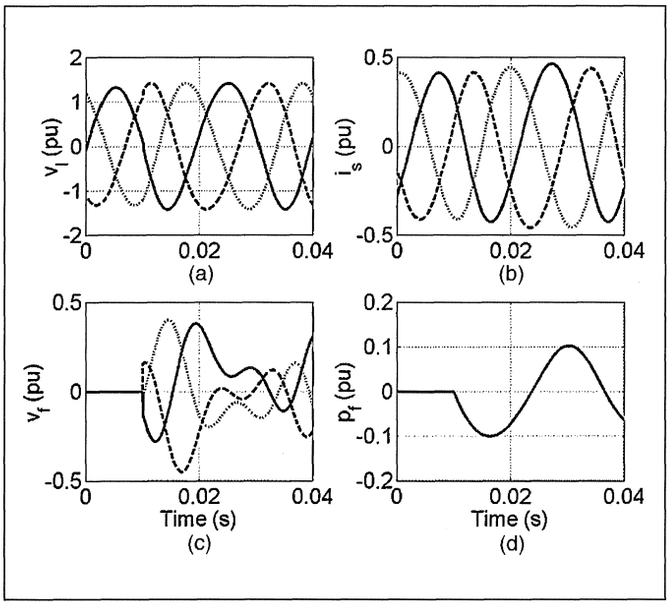

Figure 3. System performance for direct application of (7)

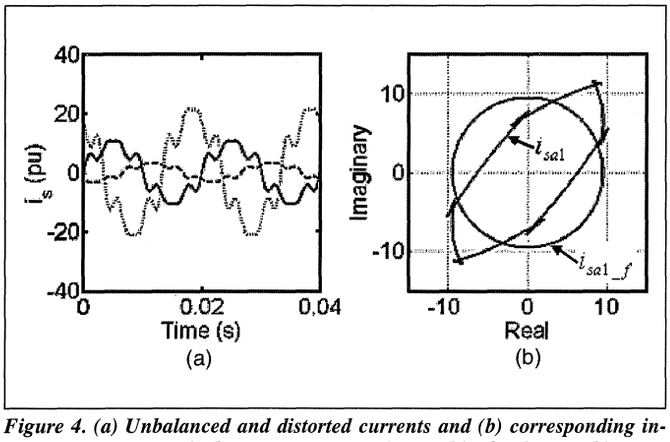

Figure 4. (a) Unbalanced and distorted currents and (b) corresponding instantaneous symmetrical component vector $i_{sa\,1}$ and its fundamental $i_{sa\,1\_f}$

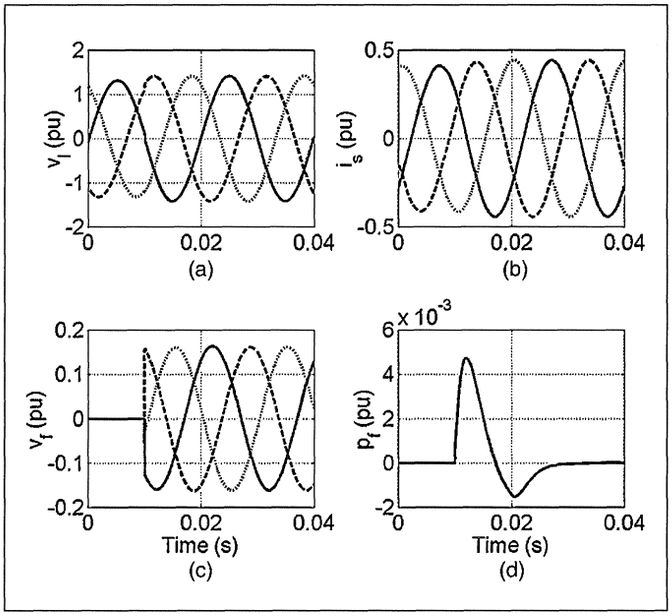

Figure 5. System performance with modified reference generation scheme