Phase Locked Loop System for FACTS

Dragan Jovcic, *Member, IEEE*

***Abstract*—This research addresses the special requirements of phase locked loops (PLLs) for a typical application with FACTS elements. A new PLL system that uses adaptation algorithms is developed with the aim of improving speed of responses, robustness to AC voltage depressions, and harmonic rejection. The adaptive PLL consists of the three control units that individually control frequency, phase angle, and voltage magnitude. The voltage controller output is used to compensate for reduced gain caused by the ac voltage magnitude depressions. The output phase angle and its derivative, the frequency signal, are controlled in two independent control systems in order to enable elimination of frequency and phase error without compromising transient responses. The simulation results are compared with a PLL available with the PSB MATLAB block-set and noticeable improvements are demonstrated. In particular, settling time and overshooting are significantly lower with conditions of reduced ac voltage magnitude.**

***Index Terms*—Frequency locked loops, modeling, phase-locked loops, power system control, thyristor circuits, tracking.**

I. Introduction

A. Background

PHASE locked loops (PLL) with all ac/dc converters take an important role in providing a reference phase signal synchronized with the ac system. This reference signal is used as a basic carrier wave for deriving valve-firing pulses in control circuits. The actual valve-firing instants are calculated using the PLL output as the base signal and adding the desired valve firings [1], [2]. Typically, the desired firings are calculated in the main control circuit achieving regulation of some output system variables. The dynamically changing reference from a PLL therefore influences actual firings and it plays an important role in the system dynamic performance.

Modern FACTS and HVDC elements have ever-increasing requirements on speed of response, performance, robustness, fault-recovery, and power quality. Their control systems are becoming sophisticated and the role of PLL structure/dynamics in meeting these requirements is becoming an important research topic [1]–[3] although it is still insufficiently investigated. Research in [1]–[3] studies the influence of PLL dynamics inside FACTS/HVDC, and [1] demonstrates that an increase in HVDC inverter PLL gains deteriorates the system stability, whereas [3] proves that *10* times reduced SVC PLL gains make responses very poor. Further in line with the above research, this paper seeks to develop a new PLL that would improve FACTS performance and that would be suitable for operating demands and conditions faced by various FACTS elements.

Manuscript received March 24, 2003.

The author is with Electrical and Mechanical Engineering, University of Ulster, Newtownabbey BT370QB, U.K. (e-mail: d.jovcic@ulster.ac.uk).

Digital Object Identifier 10.1109/TPWRS.2003.814885

Historically viewed, the first converters with transmission systems (HVDC systems) employed the individual phase firing controls using zero-crossing detection synchronizing circuits [4]. They were found to be prone to harmonic instabilities, and they were replaced with a more robust equidistant firing pulse method, employing the voltage-controlled oscillator [5]. This method has evolved to the three-phase, trans-vector-type PLL [6] that is popular with HVDC and FACTS [1]–[3], [7]. The trans-vector-type PLL has excellent internal harmonic cancellation and fairly good transient responses but it is deficient in the following: 1) Unbalanced ac voltages cause pronounced second harmonic generation, 2) Gain is reduced with lower ac voltages, 3) It is sensitive to ac voltage harmonics and speed of response must be reduced in order to prevent harmonic propagation. 4) It is unable to follow individual phase angles. Recent research [8] attempts to improve transient response of the trans-vector PLL using lead-lag compensation but the robustness, the unbalanced faults, and other issues are unresolved. Among various designs to improve robustness and positive sequence tracking, lot of praise deserves the discrete robust PLL developed with power system block-set (PSB) on MATLAB platform [9], [10] (the methodology is applied with the three-phase and single-phase PLL available as the standard unit in the PSB library in SIMULINK). This PLL design, referred here as the PSB PLL, uses the specially developed unit variable frequency average (VFA) that eliminates harmonics. It demonstrates excellent second harmonic elimination including conditions with single-phase faults and superb elimination of external ac voltage harmonics but, as shown below, it has an unfavorable transient response and very poor phase angle tracking under reduced voltages.

The desired PLL should possess generic properties: rapid response, accurate indication of unbalanced conditions, and robustness in terms of unaffected responses under voltage magnitude reduction or harmonic presence on the input ac signal.

B. Three-Phase Against Single-Phase PLL for FACTS

The design presented here can be applied to a single-phase PLL or to a three-phase configuration. Primarily, the single-phase design is addressed for the reasons presented below.

Many FACTS and HVDC converters use a three-phase PLL configuration that measures a three-phase signal (voltages or currents) and derives a single phase-reference signal. The distinct phase-references for individual phases are then calculated by adding or subtracting $2\pi/3$ radians. Such a design has the advantage of internal harmonic cancellation, but it suffers from poor representation of single-phase transients. In reality, such a PLL will give an average phase angle over three phases that poorly represents the individual phase angles.

0885-8950/03$17.00 © 2003 IEEE

In addition, in case of voltage unbalance, this PLL generates various harmonics.

A single-phase PLL gives a particular phase angle reference irrespective of the conditions on the other two phases, and therefore, allows better individual phase control of the ac system. It is presumed here that three single-phase PLL units would give a more accurate indication of the system dynamics. The central issue that has hampered single-phase PLL utilization is that a single-phase design normally generates second harmonic (there is no internal harmonic cancellation). Second harmonics in PLL are very difficult to eliminate and if eliminated, a very sluggish design typically results.

This research proposes a single phase PLL design that overcomes these obstacles and largely meets specific performance requirements as described below.

II. Design Objectives

PLLs normally use multiplication of two *sine* signals: v- the input signal, and the PLL output signal v_p, to obtain the phase error signal [11]

$$\begin{aligned} v &= V\sin(\omega t + a) \\ v_p &= V_p\cos(\omega_p t + a_p) \end{aligned} \tag{1}$$

where V, V_p are the magnitudes of the input and the PLL output, respectively, ω and ω_p are the frequencies of the input and output, and a, a_p are the phases of the input and output signal. The error signal can be derived as

$$\begin{aligned} e &= v \times v_p \\ e &= 0.5VV_p\sin\left((\omega-\omega_p)t + a - a_p\right) + \\ &\quad + 0.5VV_p\sin\left((\omega+\omega_p)t + a + a_p\right). \end{aligned} \tag{2}$$

The above error signal is processed in a feedback loop that involves filtering and a control stage. The control stage eliminates phase error, improves performance, and generates the PLL output v_p [11].

Observing (2), several specific characteristics are noted with the view of FACTS applications: 1) because of the relatively low main frequency, the second harmonic can have significant impact on the loop dynamics, 2) the loop gain is variable since ac faults reduce V, and 3) input harmonics on v can be expected to propagate through the feedback loop via V and they have frequencies that may interfere with the control loop. Additional control challenges are observed including: nonlinear gain, requirements for zero phase, but also frequency errors, and possible harmonic proliferation through the feedback loop.

Considering the practical application for FACTS and the above error signal analysis, the main design objectives are postulated:

- rapid response and zero error for the output angle and the output derivative. In FACTS applications, good phase angle but also frequency tracking are important;
- robustness to ac system voltage depressions, since it is important that PLL responses are sufficiently fast during faults and transients. Ideally, the PLL dynamic responses should be unaffected by the voltage magnitude (V) changes;

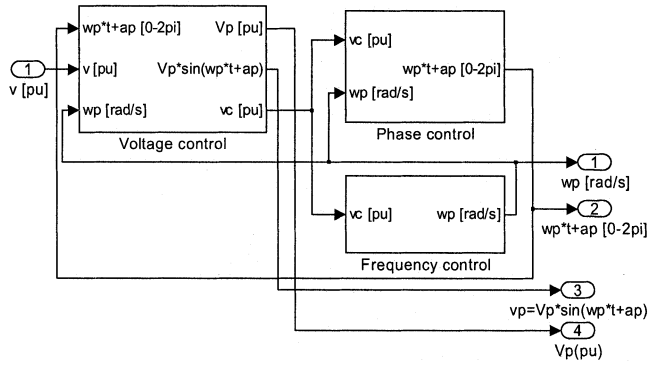

Fig. 1. PLL schematic.

- unaffected, robust response under the input ac system harmonics. These ac harmonics in the host network are a realistic expectation with the increasing use of power electronics. The harmonics on the input signal are multiplied with the feedback signal in (2), causing an array of other harmonics and nonlinear responses, depending on the system gain.
- Minimal presence of harmonics on the PLL output signal, since they can cause problems at other control levels outside the PLL. This implies total elimination of the second harmonic in (2) and filtering of any other harmonics on the input signal.

III. Adaptive PLL Structure

The underlying design assumption is that a PLL can meet the objectives only if it possesses complete information on the input signal (i.e., magnitude V, frequency ω and phase a). The proposed design generates these three components in three feedback control units. These components are used to regenerate the *sine* signal that should be a close replica of the input signal v.

Fig. 1 shows the PLL structure outlining the three main units: the voltage controller, the frequency controller, and the phase angle controller. The phase angle and the frequency controller in essence produce the same signal but in different frequency domains since $\omega = da/dt$. However, if these two signals are separately controlled and then blended in a suitably developed control loop, we are able to get very good transient responses, by means of adding two slow and robust signals. Adding two slow signals improves robustness, given that each signal is individually low-pass filtered. It is noted that in the traditional approach [6], [8], [9], a single feedback controller is used that needs to ensure good tracking of frequency and frequency integral (phase angle) and this implies a degradation in performance.

The design is labeled an adaptive PLL since the voltage control output is used to correct gain in the phase and frequency controller. The voltage controller output follows variations in the input signal magnitude, and this compensates for V in (2), in a typical adaptive control manner.

A generic control design approach for the PLL system in Fig. 1 does not exist, since it is a multivariable adaptive nonlinear system. The system is constructed by sequentially designing each of the three units as shown in the following sections.

دریافت فوری ← متن کامل مقاله

ISIArticles
مرجع مقالات تخصصی ایران

- ✓ امکان دانلود نسخه تمام متن مقالات انگلیسی
- ✓ امکان دانلود نسخه ترجمه شده مقالات
- ✓ پذیرش سفارش ترجمه تخصصی
- ✓ امکان جستجو در آرشیو جامعی از صدها موضوع و هزاران مقاله
- ✓ امکان دانلود رایگان ۲ صفحه اول هر مقاله
- ✓ امکان پرداخت اینترنتی با کلیه کارت های عضو شتاب
- ✓ دانلود فوری مقاله پس از پرداخت آنلاین
- ✓ پشتیبانی کامل خرید با بهره مندی از سیستم هوشمند رهگیری سفارشات