Selective Harmonic Elimination and Current/Voltage Control in Current/Voltage-Source Topologies: A Unified Approach

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***Abstract*—This paper presents a unified approach for generating pulsewidth-modulated patterns for three-phase current-source rectifiers and inverters (CSR/Is) that provides unconstrained selective harmonic elimination and fundamental current control. The approach uses the chopping angles or gating patterns developed for voltage-source rectifiers and inverters in combination with a logic circuit to generate the gating patterns for CSR/Is. The circuit also includes naturally and symmetrically distributed shorting pulses. Thus, the approach avoids the hassle of positioning the shorting pulses and defining and solving a set of nonlinear equations dedicated to CSR/Is. Moreover, the approach can eliminate an even or odd arbitrary number of harmonics (e.g., fundamental current control and elimination of the 5th, 7th, and 11th harmonics). This is an improvement over existing techniques and a new approach to pattern generation. Simulated and experimental results for both static and dynamic operating conditions are presented in order to validate the effectiveness of the approach.**

***Index Terms*—Current source, selective harmonic elimination, three phase, voltage source.**

I. Introduction

THREE-PHASE static power topologies can be classified as voltage-source rectifiers and inverters (VSR/Is) and current source rectifiers and inverters (CSR/Is) (see Fig. 1). The advent of switching devices with turn-off capabilities [e.g., insulated gate bipolar transistors (IGBTs), gate-turn-off thyristors (GTOs)] has made the VSRs [Fig. 1(a)] widely used for ac-to-dc conversion, in applications such as motor drives, power supplies, uninterruptible power supplies (UPSs), and static power compensators (STATCOMs). VSIs [Fig. 1(c)] have become standard in most dc-to-ac applications, such as induction and synchronous motor drives, UPS systems, and, in general, ac power supplies. Although less common, current-source topologies [Fig. 1(b) and (d)] are found in superconducting magnet energy storage (SMES) systems and in a number of industrial processes such as high-power adjustable-speed drives, where four-quadrant operation, near sinusoidal motor terminal voltages, supply voltage variations immunity, and inherent short-circuit protection are important considerations [1], [2]. The use of pulsewidth-modulated (PWM) gating patterns to control the power valves in such topologies is the base to achieve faster dynamic responses and nearly sinusoidal ac waveforms. Several PWM techniques have been reported in the literature, which can be classified as online [3]–[5] (e.g., sinusoidal PWM and space vector) or offline [6]–[9] (e.g., selective harmonic elimination and fundamental magnitude control).

Online modulation techniques have been extensively documented in the published literature. They were initially developed for VSR/Is and lately extended to CSR/Is. In fact, carrier-based techniques (for analog implementations) and space-vector-based techniques (for digital implementations) are now applicable to both configurations [5]. The appropriate gating patterns are obtained for CSR/Is based on identical principles, where the special requirements, such as the shorting pulses are provided without the hassle of calculating nor positioning them. Moreover, since the same basic principles are used, the resulting ac normalized current waveform in CSR/Is and the ac normalized voltage waveform in VSR/Is are identical. Thus, the duality between voltage and current source topologies is also extended to online implementations.

On the other hand, the elimination of low-order harmonics is an important issue in many applications where low-switching-frequency PWM patterns are required. This is the case of topologies based on CSR/Is where resonances between the input/output filter capacitance and an input/output circuit inductance may be found. As an alternative, selective harmonic elimination (SHE) techniques were introduced to provide low-order harmonic elimination in VSR/Is and recent publications have introduced generalized SHE techniques in CSR/Is [9]. In order to find the generalized patterns, the proposed approaches find the chopping angles and locate the shorting pulses by defining and solving a set of nonlinear equations dedicated to CSR/Is. Thus, fundamental current amplitude control and an even number of low-order harmonics elimination can be performed.

This work presents a new approach for generating PWM patterns for three-phase six-switch CSR/Is that provides unconstrained selective harmonic elimination and fundamental current amplitude control. The approach uses the chopping angles or

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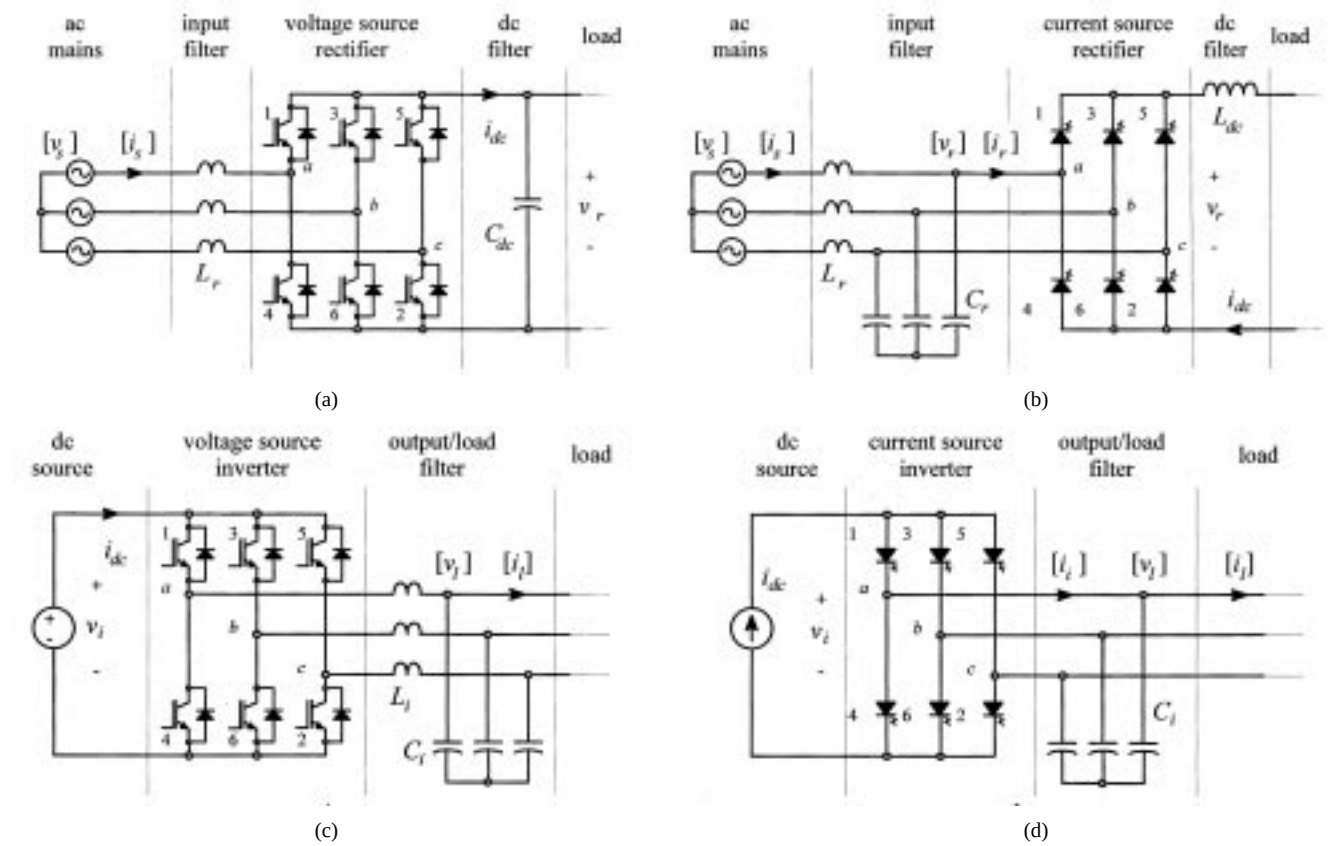

Fig. 1. Three-phase power converter topologies. (a) Voltage-source rectifier. (b) Current-source rectifier. (c) Voltage-source inverter. (d) Current-source inverter.

gating patterns developed for VSR/Is in combination with a logic circuit to generate the gating patterns for CSR/Is. The circuit also includes naturally and symmetrically distributed shorting pulses. Contrary to existing techniques, the approach avoids the hassle of positioning the shorting pulses and defining and solving a set of nonlinear equations dedicated to CSR/Is. Moreover, the proposed approach can eliminate an even or odd arbitrary number of harmonics (e.g., fundamental current control and elimination of the 5th, 7th, and 11th harmonics) without any penalties in the switching frequency. Simulated and experimental results are presented to validate the effectiveness of the approach.

II. Selective Harmonic Elimination in VSR/Is

The chopping angles for three-phase VSRs [Fig. 1(a)] and VSIs [Fig. 1(c)] are specified between 0–$\pi/2$ to eliminate an even number of low-frequency harmonics (e.g., 5th and 7th) and between 0–$\pi/3$ to eliminate an odd number of low-frequency harmonics (e.g., 5th, 7th, and 11th), which allow maximum dc voltage utilization. The line-to-neutral PWM patterns were named TLN1 and TLN2 as stated in [8]. For instance, to eliminate the 5th and 7th harmonics and perform fundamental magnitude control, the TLN1 pattern is used, where three angles are required (N = 3). Thus, $N-1=2$ and the equations to be solved, as indicated in [6], are

$$\begin{aligned}\cos(1\alpha_1)-\cos(1\alpha_2)+\cos(1\alpha_3)&=(2+m\pi)/4\\ \cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3)&=1/2\\ \cos(7\alpha_1)-\cos(7\alpha_2)+\cos(7\alpha_3)&=1/2\end{aligned}\tag{1}$$

where the angles α_1, α_2, and α_3 are defined as shown in Fig. 2 and m is the modulation index (amplitude of the fundamental phase voltage component for a 1-pu dc-link voltage). The angles α_1, α_2, and α_3 are plotted for different values of the line voltage fundamental amplitude component [$m\sqrt{3}$ in Fig. 3(a)] assuming 1–pu dc-link voltage. The general expressions to eliminate $N-1$ ($N-1=2,4,6,\cdots$, even) harmonics were derived in [8] and are given by the following equations:

$$\begin{aligned}-\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k)&=\frac{2+m\pi}{4}\\ -\sum_{k=1}^{N}(-1)\cos(n\alpha_k)&=\frac{1}{2},\qquad \text{for } n=5,7,\cdots,3N-2\end{aligned}\tag{2}$$

where $\alpha_1, \alpha_2,\cdots,\alpha_N$ should satisfy $\alpha_1 < \alpha_2 < \cdots < \alpha_N < \pi/2$.

Similarly, to eliminate an odd number of harmonics, for instance, the 5th, 7th, and 11th, and perform fundamental magnitude control, the TLN2 pattern is used. Thus, $N-1=3$ and the equations to be solved, as indicated in [6], are

$$\begin{aligned}\cos(1\alpha_1)-\cos(1\alpha_2)+\cos(1\alpha_3)-\cos(1\alpha_4)&=(2-m\pi)/4\\ \cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3)-\cos(5\alpha_4)&=1/2\\ \cos(7\alpha_1)-\cos(7\alpha_2)+\cos(7\alpha_3)-\cos(7\alpha_4)&=1/2\\ \cos(11\alpha_1)-\cos(11\alpha_2)+\cos(11\alpha_3)-\cos(11\alpha_4)&=1/2\end{aligned}\tag{3}$$