A Unique Fault-Tolerant Design for Flying Capacitor Multilevel Inverter

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***Abstract*—This paper presents a unique design for flying capacitor type multilevel inverters with fault-tolerant features. When a single-switch fault per phase occurs, the new design can still provide the same number of converting levels by shorting the fault power semiconductors and reconfiguring the gate controls. The most attractive point of the proposed design is that it can undertake the single-switch fault per phase without sacrificing power converting quality. Future more, if multiple faults occur in different phases and each phase have only one fault switch, the proposed design can still conditionally provide consistent voltage converting levels. This paper will also discuss the capacitor balancing approach under fault-conditions, which is an essential part of controlling flying capacitor type multilevel inverters. Suggested fault diagnosing methods are also discussed in this paper. Computer simulation and lab results validate the proposed controls.**

***Index Terms*—Flying capacitor, multilevel inverters, single-switch fault.**

I. Introduction

THE HEART of many modern dc/ac inverter designs include multilevel concept, which improves the power quality by inserting a number of small voltage steps in the line-to-ground voltages. Lower losses and improved electromagnetic current (EMC) are additional benefits of multilevel converters [1]–[7]. The main disadvantage of multilevel converters is that they require more power semiconductors. Most studies on multilevel inverters are focused on the topology and control aspects, with some focus on fault-tolerance [8]–[13]. Fault-tolerance is an important area considering reduction of downtime in industrial processes and survivability of Naval ship propulsion systems. [14]–[18] discuss the fault issue of common two-level converters from different aspects. When typical two-level inverters are applied to a safety-critical system, duplex or even triplex redundant models can be used to handle the fault situation. However, this can be an impractical solution for most multilevel inverters due to cost and size concerns. Nevertheless, redundancy, which can be viewed from several different aspects, is still the crux in designing fault-tolerant systems. Even though providing duplex or triplex redundant multilevel converter models is not an ideal solution, another type of redundancy, topology configuration redundancy, highlights a direction for designing the multilevel inverter system with fault-tolerant features. A multilevel inverter system has this type of redundancy available if its topology has several different switching configurations for generating the same numbers of line-to-ground voltage levels. The diode-clamped multilevel inverter (DCMI) [1], [2] and the flying capacitor multilevel inverter (FCMI) [3], [4] are two of the most popular multilevel inverter topologies. [8]–[12] discuss the fault-tolerant features of the DCMI and FCMI, which present fault-tolerant solutions by sacrificing some of the converting levels when a fault occurs. This paper will present a unique solution for the four-level fault-tolerant multilevel inverter which can keep consistent converting levels even under single-switch fault per phase conditions. Compared to DCMI, FCMI topology has more switching state redundancy per voltage converting level and the large number of redundant voltage levels allows extra opportunities for capacitor voltage balancing [7]. Therefore, the FCMI topology is adopted in this fault-tolerant design.

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II. Three-Cell Four-Level FCMI Topology Review and its Topology Redundancy

Fig. 1(a) shows a three-cell four-level FCMI connected to a three-phase electrical machine. The line-to-ground voltage of the xth phase can be expressed as

$$v_{\mathrm{xg}} = \frac{s_x}{3} v_{\mathrm{dc}}, \quad s_x = 0, 1, \ldots 3 \tag{1}$$

where x represents the phase a, b, or c, and s_x represents the phase switching states selected by the gating signals. The line-to-neutral voltages are given by [19]

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{\mathrm{cs}} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}. \tag{2}$$

The conventional m-cell FCMI topology [2], where each cell includes one dc source and one pair of complementary switches, sets dc voltages to

$$v_{\mathrm{xi}} = \frac{i}{m} v_{\mathrm{dc}}, \quad (i = 1, 2, \ldots m). \tag{3}$$

This voltage setting yields $n = m + 1$ line-to-ground voltage levels. Specifically, the three-cell FCMI as shown in Fig. 1 sets dc voltage ratio as v_{x1}:v_{x2}:v_{x3} = 1:2:3, which yields four line-to-ground voltage levels. Recent research shows that different line-to-ground levels may be obtained by varying the dc link voltage ratio settings. A new full binary combination scheme (FBCS) is reported in [4], which covers the maximum

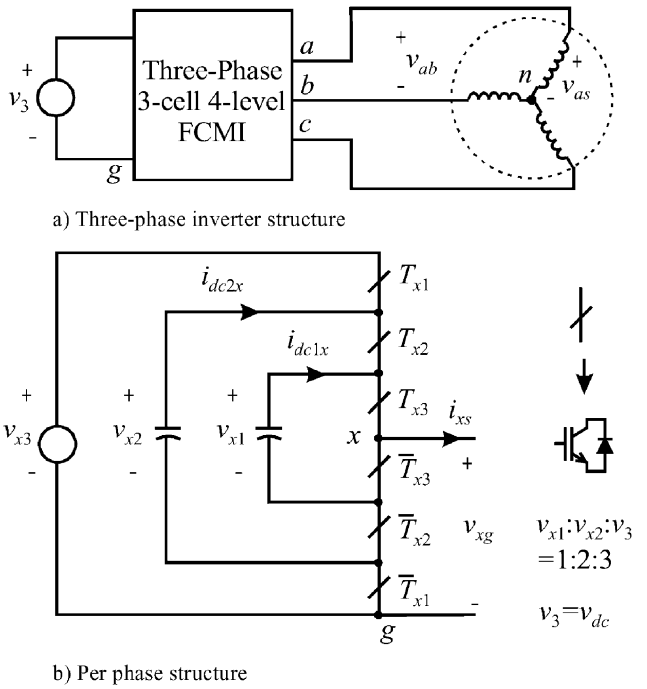

Fig. 1. Three-cell four-level flying capacitor topology.

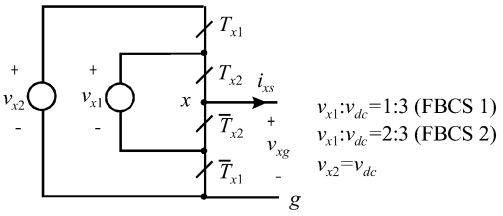

Fig. 2. Two-cell four-level floating voltage source inverter topology.

TABLE I
TWO-CELL FOUR-LEVEL FBCS INVERTER

	T_{x1}	T_{x2}	s_x	v_{xg}
FBCS 1,2	0	0	0	0
FBCS 1	0	1	1	$v_{dc}/3$
FBCS 2	1	0		
FBCS 1	1	0	2	$2v_{dc}/3$
FBCS 2	0	1		
FBCS 1,2	1	1	3	v_{dc}

switching state combinations thus generating more converting levels.

FBCS 1 sets dc voltages to

$$v_{\mathrm{xi}} = \left(\frac{2^i - 1}{2^m - 1}\right) \cdot v_{\mathrm{dc}}. \tag{4}$$

FBCS2 sets dc voltages to

$$v_{\mathrm{xi}} = \left(1 - \frac{2^{m-i} - 1}{2^m - 1}\right) \cdot v_{\mathrm{dc}}. \tag{5}$$

Both FBCS 1 and FBCS 2 result in 2^m levels of v_{xg}. According to FBCS, a two-cell FCMI as shown in Fig. 2 can generate four line-to-ground voltage converting levels either by setting the voltage ratio to v_{x1}:$v_{\mathrm{x2}} = 1$:3 (FBCS 1) or 2 : 3 (FBCS 2). Table I shows the switching states and the related line-to-ground voltage converting levels. Note that the three-cell four-level FCMI topology as shown in Fig. 1(b) actually includes the two-cell four-level FBCS topologies. Suppose that the capacitors are balanced, when one takes the v_{x2} dc branch out from the three-cell topology and forces T_{x1} and T_{x2} open or closed together, it will be identical to the topology shown in Fig. 2 with v_{x1}:$v_{\mathrm{x2}} = 1$:3. Similarly, if one takes the v_{x1} dc branch out from the three-cell topology and force T_2 and T_3 open or closed synchronously, it will be identical to the topology shown in Fig. 2 with v_{x1}:$v_{x2} = 2$:3. The two-cell FBCS configurations can be treated as the topology configuration redundancies of the conventional three-cell FCMI. This new discovery has a very special meaning to the fault-tolerant design of the three-cell four-level multilevel inverter. When single switch fault happens, if one can reconfigure the switching connections and gate controls so as to acquire an equivalent two-cell FBCS topology as well as the effective capacitor balancing approach, then the inverter can always provide four line-to-ground voltage levels. This paper will present such a fault-tolerant inverter design which may provide four consistent line-to-ground converting levels even under single-switch-per-phase fault situation. For clarity, Section III will focus on the discussion of the circuitry reconfiguration under fault conditions with the assumption that the dc capacitor voltages have no balancing problem. Section IV will release the assumption for discussing the dc capacitor voltage balancing approach and related controls. Computer simulation studies and lab validation are included in Sections V and VI, respectively.

III. FAULT ANALYSIS FOR THE THREE-CELL FOUR-LEVEL FCMI

A. Single Switch Faults

The three-cell FCMI topology, as shown in Fig. 1, includes three pairs of complementary power semiconductors in each phase. No matter which semiconductor is faulted, it is always possible to reconfigure the inverter topology to make it work as a two-cell FBCS inverter, which can still guarantee four line-to-ground converting levels. For instance, when a T_{x1} fault is detected, one may bypass the fault semiconductor T_{x1} and force $\bar{T}_{\mathrm{x1}}$ to be closed, and at the same time separate the v_{x2} branch from the main circuitry. Then equivalently, v_{x1} branch, v_{x3} branch, T_{x2}, $\bar{T}_{\mathrm{x2}}$, T_{x3}, and $\bar{T}_{\mathrm{x3}}$ form a two-cell four-level FBCS inverter phase leg. This inverter will work under the configuration of two healthy three-cell FCMI phase legs and one equivalent two-cell FBCS phase leg, which can still provide four voltage-converting levels. Table II lists the related actions taken under the different fault cases. Fig. 3 shows all the possible circuitry configurations for the six single-switch-fault cases per phase.