A New Reliability Evaluation Technique for Multi-Level Inverters

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***Abstract*— Multi-level inverters play a key role in today's micro grids with renewable energy sources. The reliability of multi-level inverters, as the interface of renewable units, has critical impacts on providing electricity requirement of the customers connected to the grid. Therefore, this paper presents a new reliability evaluation technique for multi-level inverters. The method is on the basis of the state enumeration approach. Unlike the previous methods, the new approach engages harmonic distortion levels produced by the inverter in the reliability index calculation. Without loss of generality, only single failure of capacitors and semiconductor switches are considered here which can be easily extended to incorporate the other elements. Employing the developed technique, one can estimate the reliability of various multi-level topologies and hence, make her decision by compromising between reliability, efficiency, and investment cost. In the simulations, a set of reliability indices for several multi-level inverter topologies are computed to demonstrate the effectiveness of the proposed approach.**

Keywords*— *Harmonic distortion, multi-level inverter, reliability evaluation.

I. INTRODUCTION

Today, micro grids are known as the solution to relieve the future energy crisis and reliability concerns. A typical micro grid comprises of a set of generating units, a set of energy storage devices, and loads. A micro grid can provide the customers electrical energy even when the main grid is disconnected. The generating units in a micro grid are usually in type of renewable energy sources. These renewable units are also commonly connected to the network by inverters. The limitations of present semiconductor technologies coupled with the consequences of harmonic distortions are the main driving forces for implementation multi-level inverters [1].

To date, various topologies for multi-level inverters have been proposed and surveyed in the literature [2]-[5]. These topologies have particular pros and cons that must be taken into account at the time of selection. Amongst, the reliability and no load consumption, i.e., efficiency, are the most important ones. The efficiency of different multi-level inverter topologies has been investigated in the literature. Reference [1] has explored the conceptual basis of commonly used multi-level inverters. It has provided a detailed comparison between the efficiency of different topologies as well. An appropriate method for reliability evaluation of three-level inverters has been proposed in [6]. The developed method is on the basis of the multi-state systems' concept [7]. Although the harmonic levels produced by the inverters are critical factors for proper functioning of the grid, they are not considered in method developed in [7]. This paper extends the reliability evaluation technique presented in [7] to encompass the grid sensitivity in response to generated harmonics. In the developed method, possible system states are selected through the state enumeration approach [8]. In the simulations, similar to [7], only single failure of capacitors and semiconductor switches are considered in this paper.

Using the developed method, reliability of a specific multi-level inverter is calculated considering to the characteristics of the served electricity loads. Therefore, the reliability indices derived from the presented technique depend on both the inverter topology and load characteristics. Synonymously, similar multi-level inverters are more reliable when the loads are harmonic insensitive compared to the case in which electricity loads are harmonic sensitive.

Moreover, the proposed technique can be useful for one who wishes to select a multi-level inverter among different topologies. He compares the reliability of different inverter topologies considering the application, i.e., behavior of the loads. Thereafter, he makes the decision by compromising between reliability, efficiency, and investment cost.

To demonstrate the effectiveness of the proposed methodology, a set of commonly used multi-level inverters covering cascade H-bridge, diode-clamped, flying capacitor, modular, and multiple source topology are implemented. The reliability indices for the mentioned inverters are compared for various applications with different load characteristics.

The paper organization is as follows. Section II reviews the commonly used multi-level inverter topologies. The proposed methodology is presented in Section III. Simulation results and discussions are addressed in Section IV. Conclusions are drawn in Section V.

II. COMMON TOPOLOGIES FOR MULTI-LEVEL INVERTERS

As mentioned heretofore, various topologies for multi-level inverters have been proposed in the literature. All of them have particular advantages and disadvantages. A brief review on the most commonlly used topologies is provided in the following sections.

A. Cascade H-Bridge Topology

The single line diagram of a five-level cascade inverter is

shown in Fig. 1. In this structure, a set of separate DC voltage sources is required each of which is connected to a H-bridge inverter. Three different voltage levels including +V, -V, and 0 can be generated by each H-bridge inverter via different combinations of switch statuses. In cascade H-bridge topology, the AC outputs of the mentioned H-bridge inverters are connected in series. In such a situation, the final output AC waveform is the sum of the inverter outputs. Using cascade H-brigde topology, the total number of output voltage levels is equal to the number of cascaded H-bridges multiplied by two plus one. Finally, requirement of a separate DC source for each H-bridge inverter is the major disadvantage of this structure.

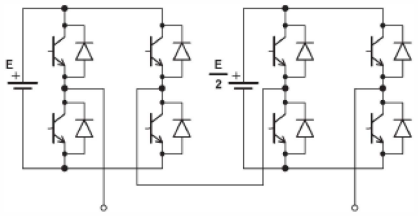

Figure 1. Single line diagram of a five-level inverter with cascade H-bridge topology.

B. Diode-Clamped Topology

The diode-clapmed multi-level inverter topology was proposed in 1981 by Nabaei et al [9]. The single line diagram of a five-level diode-clamped inverter is shown in Fig. 2. In this structure, a DC voltage source is sub-divided into some voltage levels by a set of similar capacitors. As shown in Fig. 2, each single-phase diode-clamped inverter consists of two legs. By different combinations of switch statuses, three different voltage levels covering +V/2, -V/2, and 0 can be generated by each leg of the diode-clamped inverter. In this structure, the AC output voltage consists of left-side leg voltage and right-side leg voltage. In such a situation, the final output AC waveform is the subtract of the legs' voltages. Using diode-clapmed topology, the total number of output voltage levels is equal to the number of series switches in each leg plus one. Finally, capacitor voltage balacing is the major disadvantage of this structure.

C. Flying Capacitor Topology

The flying capacitor multi-level inverter topology was proposed in 1992 by Meynard et al [10]. The single line diagram of a five-level flying capacitor inverter is illustrated in Fig. 3. In this structure, role of flying capacitors is similar to that of the clamping diods in previous topology. Implementing capacitors instead of clamping diods enables the inverter to ride through short duration outages and deep voltage sags. However, flying capacitor inverters are more expensive and bulky than diode-clamped inverters. Finally, similar to the case of diode-clamped topology, capacitor voltage balacing is one of the serious disadvantages in flying capacitor inverters.

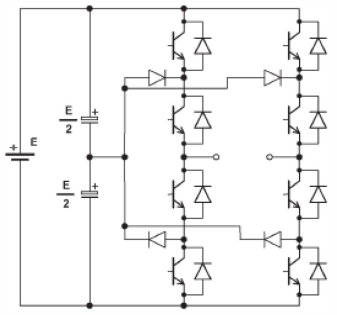

Figure 2. Single line diagram of a five-level inverter with diode-clamped topology.

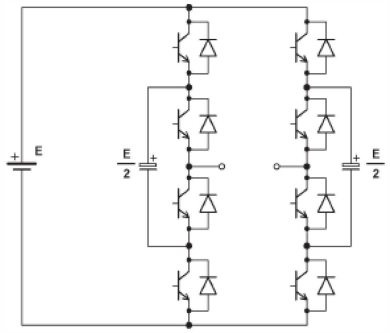

Figure 3. Single line diagram of a five-level inverter with flying capacitor topology.

D. Modular Topology

The single line diagram of a modular multi-level inverter is depicted in Fig. 4. This structure has been recently proposed for high power applications in [11]-[12]. Modular multi-level inverters are very cost-effective mainly because of their stringent modular construction. However, capacitor voltage balacing is one of the main disadvantages in multi-level inverters with modular topology.

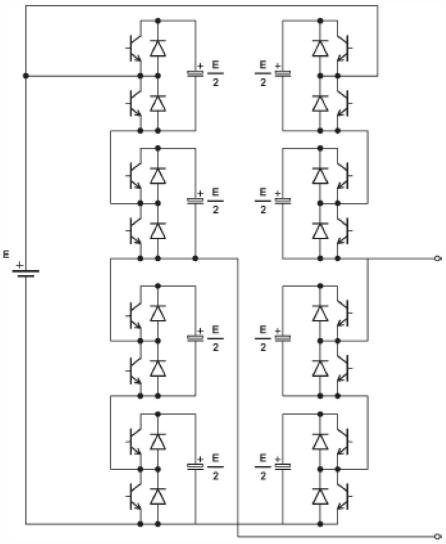

Figure 4. Single line diagram of a five-level inverter with modular topology.

E. Multiple Source Topology

The single line diagram of a multiple source multi-level