Cancellation and Attenuation of Harmonics in Low Voltage Networks

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***Abstract*—Increasing numbers of various power electronic equipment, used both as passive devices (e.g. front-end rectifier loads) and as active devices (e.g. inverter-interfaced generation), is one of the main contributing factors to the higher harmonic distortion levels in low voltage distribution networks. The analysis and results presented in this paper discuss and demonstrate how modern power electronic devices interact with each other and with the low voltage network. To represent the effects of harmonic cancellation and harmonic attenuation, different types of power electronic equipment are analysed for several characteristic system impedance values and typically distorted voltage waveforms.**

Keywords—harmonic attenuation; harmonic cancellation; power electronic devices; power quality, system impedance; voltage waveform distortion.

I. INTRODUCTION

Growth in numbers of various types of power electronic equipment, used both as passive devices (e.g. front-end rectifier loads) and even more as active devices (e.g. inverter-interfaced generation), is one of the main factors contributing to both increased power demands and higher harmonic distortion levels in low voltage (LV) networks.

This paper investigates how different types of modern power electronic devices interact with each other and with the LV network. These interactions are represented and quantified through the analysis of harmonic cancellation and harmonic attenuation effects (in the frequency range up to 3 kHz), which are assessed by calculating/simulating and measuring harmonic contents (magnitudes and phase angles of harmonics) and total harmonic distortion (THD) levels. The analysis includes different types of power electronic equipment, several characteristic system impedance values and some typically distorted voltage waveforms encountered in LV networks.

II. MODELLING FRAMEWORK

Recent statistics estimate that the combined contribution of various types of power electronic loads is currently responsible for about 30-35% of the total electricity demand in the UK residential load sector [1] A significant part of that demand is due to power electronic loads utilising switch-mode power supply (SMPS) circuit (used for the conversion of the ac supply voltage to a regulated dc voltage in a wide range of end-use applications, from televisions, set-top boxes and different audio/visual equipment, to printers, modems and desktop computers), as well as due to energy efficient lighting loads utilising an electronic ballast (used for the control and operation of modern compact fluorescent lamps, CFLs). The operation of both SMPS and CFL loads will result in an input ac current waveform which has a rich harmonic content. To allow for better control of harmonic emissions, all single-phase loads with rated currents below 16 A connected to LV networks in the EU must satisfy harmonic legislation in [2].

As a consequence of stipulated harmonic emission limits in [2], all SMPS loads can be divided into three general (i.e. generic) types: SMPS loads with no power factor correction circuit (no-PFC loads, with rated power less than or equal 75 W), SMPS loads with passive power factor correction circuit (p-PFC loads) and SMPS loads with active power factor correction circuit (a-PFC loads), both with rated powers typically greater than 75 W. Because of the differences in their electrical characteristics, no-PFC, p-PFC and a-PFC types of SMPS loads should be represented with three different electrical models. On the other hand, typical CFL loads in residential applications are generally with rated powers less than or equal 25 W (limit for "Class C" lighting load in [2]), allowing to use only one general (i.e. generic) type and model of CFL loads for the analysis of their electrical characteristics.

This section concentrates on modelling no-PFC and p-PFC types of SMPS loads, as well as CFL loads. The simulation framework implemented in this paper can be divided into three main stages: a) modelling of individual generic load types, b) modelling of LV network, and c) Monte Carlo simulations for representing aggregate loads in LV networks.

A. Modelling of individual generic load types

Previous analysis in [3]-[6] has shown that both no-PFC and p-PFC SMPS loads, as well as CFL loads, can be represented by an equivalent circuit model given in Fig. 1. This model consists of a diode bridge rectifier, dc link capacitor C_{dc}, input impedance (denoted as R_{total} and L_{total}, representing the sum of all series impedances in the front-end rectifier circuit) and an equivalent variable resistance r_{eq}.

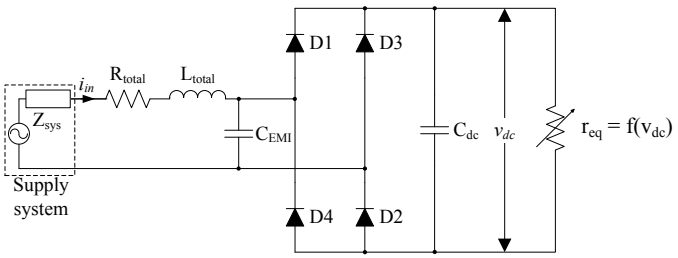

Fig. 1. Equivalent circuit model of SMPS and CFL loads.

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In Fig. 1, the EMI filter is represented by one equivalent capacitor C_{EMI} and is normally not included in the load model, as its value is very small. Consequently, the equivalent circuit CFL/SMPS model requires only three parameters: total input impedance, dc link capacitance and a variable equivalent resistance. The equivalent circuit model is further dependent on the power demand at the dc link (fluorescent tube power in the case of CFL and actual dc load for SMPS).

The value of equivalent resistance is determined by an analytical expression, which describes the behaviour of all circuit components connected to the right of C_{dc} (i.e. the circuit components used for dc voltage regulation and the dc load itself) as a function of the dc link voltage v_{dc}.

In case of the SMPS load and for a given operating condition (i.e. given dc load), the dc-dc converter will supply constant voltage and constant current to the dc load. This will result in constant power being drawn from the dc link. Therefore, the equivalent resistance can be expressed as:

$$r_{eq} = v_{dc}^2 / P_{dc} \tag{1}$$

where: v_{dc} is instantaneous dc link voltage in V, and P_{dc} is dc power demand of the SMPS load for given operating condition in W.

In the case of CFL loads, the average power drawn by the fluorescent tube, P_{tube}, can vary between approximately 0.87-1.02 pu, with respect to the rated power of the CFL at nominal supply ac voltage. These variations are included in the equivalent circuit CFL model by modifying the equivalent resistance, (3) – (4), using a per-unit conversion α (5):

$$R_{eq,discharging} = (24.5 v_{dc} + 94.29)\alpha \tag{3}$$

$$R_{eq,charging} = \left(0.01928 v_{dc}^2 + 11.69 v_{dc} + 1110\right)\alpha \tag{4}$$

$$\alpha = V_{rms}^4 / 11 P_{CFL} \tag{5}$$

where: v_{dc} is instantaneous dc link voltage in V, $R_{eq,charging}$ and $R_{eq,discharging}$ are equivalent resistances during charging and discharging stages of the dc link capacitor, respectively, in Ω, and P_{CFL} is the rated power of the CFL in W.

Equivalent circuit parameter values for the two considered types of SMPS loads and CFL load type are given in Table I. The typical/mean parameter values for each type of the load (denoted as "μ") are identified by inspection of actual devices, review of manufacturers datasheets, parameter fitting to the measured data and more detailed simulation of important electrical characteristics. This approach also allowed identification of the distributions of model parameter values (e.g. normal or uniform), as well as the range of variations of parameter values found for specific type of modelled power electronic load due to, e.g., differences in electronic circuits between different manufacturers, or actual tolerances of values of specific circuit components (denoted as "standard deviations σ"). Identification of these typical values and ranges of their variations is important for the correct simulation of a large number of these devices when they form an aggregate demand (see Section II.C, with further details provided in [3]-[6]).

TABLE I. PARAMETER VALUES FOR THE EQUIVALENT CIRCUIT MODEL

Load	Parameter	Distribution	Values (pu)
no-PFC SMPS	X_{Cdc}	Normal	μ = 0.036, σ = 0.54
	R_{total}	Uniform	[0.0015, 0.0019]
	X_{Ltotal}	Uniform	[2.97 x 10^{-6}, 8.91 x 10^{-6}]
	P_{dc}	Normal	μ = 0.5, σ = 0.16
p-PFC SMPS	X_{Cdc}	Normal	μ = 0.036, σ = 0.54
	R_{total}	Uniform	[0.0077, 0.0094]
	X_{Ltotal}	Normal	μ = 0.0371, σ = 0.0019
	P_{dc}	Normal	μ = 0.5, σ = 0.16
CFL	X_{Cdc}	Normal	μ = 0.25, σ = 3.75
	R_{total}	Uniform	[0.9, 1.1]
	X_{Ltotal}	Constant	3.92 10^{-5}
	P_{tube}	Uniform	[0.87-1.02]

B. Network modelling

The system impedance model used in this paper to represent the LV supply network is shown in Fig. 2.

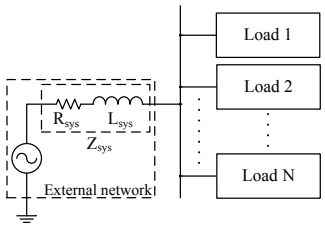

Fig. 2. Single-line equivalent of aggregate load connected to the LV network.

The value of system impedance will vary throughout the network, but some guidance on the expected values for LV residential customers is available in [7]. The values from [7], which are used along with an assumed minimum value from [6], are listed in Table II, where 'stiff grid' represents very strong LV network with system impedance equal to zero.

TABLE II. SYSTEM IMPEDANCE VALUES [6, 7]

Value	System impedance (Ω)	R (Ω)	L (mH)
Min	0.12 + j0.11	0.12	0.35
Nom	0.25 + j0.23	.25	0.73
Max	0.46 + j0.45	0.46	1.43
Stiff	0 +j0	0	0

The values of Z_{sys} in Table II include both the impedance of the LV network and the single-phase service cable, which connects individual households to the LV network. As the impedance of the service cable is relatively high, it is assumed to dominate the system impedance seen by individual household loads. Therefore, the system impedance values are shared by the different loads connected to the supply system, and this value is proportionally reduced to allow for a realistic representation of system impedance in presented simulations. Furthermore, a total of seven power electronic devices per household was assumed, based on the available device ownership statistics, e.g. [1] in the UK, so the value of system impedance is proportionally reduced for every seven appliances connected to the LV network model.

C. Monte Carlo simulation approach

In order to assess the effect of the different types of SMPS and CFL loads on the THD levels in LV networks, a number of these loads are simulated with model parameters allowed to