Fault-Tolerant Neutral-Point-Clamped Converter Solutions Based on Including a Fourth Resonant Leg

Salvador Ceballos, Josep Pou, *Member, IEEE*, Jordi Zaragoza, *Student Member, IEEE*, Eider Robles, José Luis Villate, and José Luis Martín, *Member, IEEE*

***Abstract*—This paper presents a new three-level topology based on the neutral-point (NP)-clamped converter. An additional leg is added to the basic topology. The main purpose of this leg is to provide the converter with fault-tolerant capabilities. In addition, during normal operation mode, the fourth leg can be used to balance the NP voltage. In this way, the low-frequency voltage oscillations that appear in the NP under some operating conditions are cancelled out effectively. As a result, the modulation strategy of the three main legs of the converter does not have to take care of the voltage balance and can focus on other aspects such as, for instance, minimizing the switching losses of the converter. However, the inclusion of the fourth leg produces some additional losses. A resonant topology is proposed to minimize the switching losses of this leg. Three different fault-tolerant solutions based on the fourth-leg topology are presented. A comparison of these topologies showing their respective advantages and drawbacks is made. Experimental results are presented to show the viability of this approach.**

***Index Terms*—Efficiency, fault tolerance, multilevel converter, neutral-point (NP)-clamped (NPC) converter, reliability, resonant converters, voltage oscillation.**

I. Introduction

THE use of multilevel converter has been continuously increasing over the last years [1]–[4]. Traditionally, these converters were used in medium-voltage and high-power applications. Nowadays, however, their use in low-power applications seems also to be very promising [5], [6].

This higher utilization of multilevel converters is a direct consequence of the advantages derived from their use. Perhaps, the most important of these advantages is their ability to handle high voltages, while semiconductor devices have to withstand only a portion of those voltages. Other important advantages of these converters are the low harmonic distortion of the voltages and currents, the small size of the required filter elements, the limitation of voltage transients dv/dt, the high efficiency across the whole power operation range, and the reduced common-mode voltages.

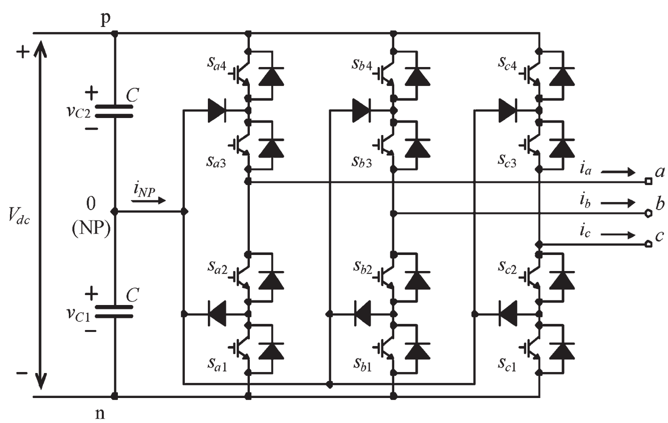

Fig. 1. NPC converter.

In the last three decades, several multilevel converter topologies have been developed. Among them, the three most important are the diode-clamped converter [7], [8], the flying-capacitor converter [9], and the cascade connection of H bridges [10]. Theoretically any number of voltage levels can be achieved with these topologies. However, due to practical limitations, the three-level versions of these converters are the most often used, particularly the diode-clamped converter type commonly known as neutral-point (NP)-clamped (NPC) converter (Fig. 1).

An important concern in this topology, which has been deeply studied in recent years, is how to keep the NP voltage at one-half of the dc link. Unfortunately, there are some operating conditions under which low-frequency voltage oscillations or even instabilities appear at the NP [11]–[13]. This fact means that the power devices and dc-link capacitors have to be oversized.

Additionally, fault tolerance is becoming more and more important in many applications. This is particularly significant in multilevel converters because the possibility of failure is higher as the number of switches increases. Consequently, the reliability of the system decreases [14].

Several solutions have been recently presented with the aim of overcoming this problem. In [15]–[17], possible solutions applied to the floating-capacitor converters are presented. In

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S. Ceballos, E. Robles, and J. L. Villate are with the Energy Unit, Tecnalia Research and Innovation, 48160, Derio, Spain (e-mail: Salvador.ceballos@tecnalia.com; eider.robles@tecnalia.com; joseluis.villate@tecnalia.com).

J. Pou and J. Zaragoza are with the Terrassa Industrial Electronics Group, Department of Electronic Engineering, Technical University of Catalonia, 08222 Terrassa, Spain (e-mail: pou@eel.upc.edu; zaragoza@eel.upc.edu).

J. L. Martín is with the Applied Power Electronics Research Team, Department of Electronics and Telecommunication, University of the Basque Country, 48013 Bilbao, Spain (e-mail: joseluis.martin@ehu.es).

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[18], a solution is applied to the converter with a generalized topology, and in [19]–[21], fault-tolerant solutions are applied to cascade converters.

Lastly, some solutions applied to the diode-clamped converter are proposed in [22]–[32]. These solutions can be classified into two major groups. First, there are those solutions based on three-legged topologies [22]–[27]. These solutions are quite simple, but unfortunately, they have some disadvantages. For example, in the case of a switch break, the modulation index of the converter has to be reduced, and therefore, the amplitude of the output voltages diminishes. As a result, these solutions are not well suited to work on grid-connected applications in which the converter normally operates under a modulation index close to the maximum. A solution to this problem is proposed in [28]. However, in this case, the semiconductors have to be able to withstand the total dc-link voltage. Consequently, this solution is only useful for low-voltage and low-power applications.

Second, some other solutions based on four-legged converters have been presented [29]–[32]. These topologies are more complex than the previous ones. Nevertheless, some of them keep all the advantages derived from the use of multilevel converters even after a switch-fault event. Moreover, some of these topologies include additional degrees of freedom which help to improve the converter performance during normal operating conditions (without semiconductor failures). The multilevel converter presented in this paper is included in this category. It is a four-legged topology whose main purpose is to endow the system with fault-tolerant capabilities. In the case of a switch failure, the additional leg will replace the damaged phase, thus increasing the reliability of the system.

Moreover, during normal operating conditions, the fourth leg can help in achieving a reliable NP voltage, removing the low-frequency NP voltage oscillations completely. In addition, because it is no longer necessary to take care of the NP voltage balance, the modulation strategy can be focused on other aspects, such as maximizing the efficiency of the topology. This can be achieved by using a modulation strategy for the three main legs of the converter that reduces the switching losses. Moreover, in order to minimize the power losses caused by the fourth leg, a resonant structure is introduced, which guarantees that the switching events in this leg are produced either under zero-voltage or zero-current principle.

This paper is an extension of the ideas presented in [30] and [31]. Two additional fault-tolerant solutions are introduced. Experimental results and practical considerations regarding the reliability and cost of each solution are also shown. This paper is divided into two main blocks. The first one includes Sections II–IV and describes the topology proposed and some modulation and control strategies for the converter when it is operating in the absence of failures. The second part, which corresponds to Sections V and VI, presents and analyzes three different fault-tolerant solutions based on the basic four-leg topology presented before.

II. Topology Proposed

Fig. 2 shows a basic scheme of the topology presented in this paper. It can be observed that, in addition to the three main legs of a standard NPC converter, there is a fourth leg connected to the NP of the converter through an inductance. This Section gives a brief explanation about how this topology works under normal operating conditions. A more detailed explanation can be found in [30].

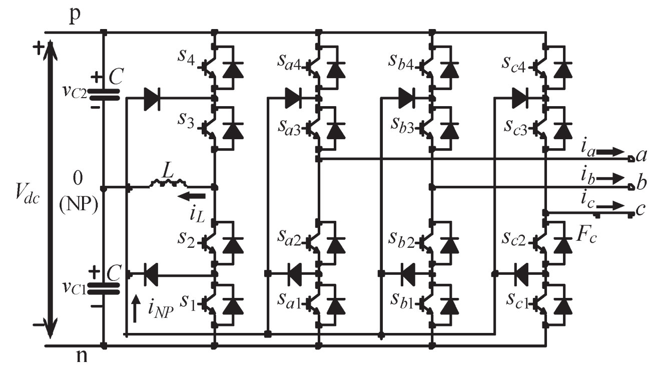

Fig. 2. Proposed topology.

TABLE I
Switching States of the Fourth Leg

i_L>0	Action
1	Turn on S_3 and S_4 if t< t_{on} Turn off all the switches when t>t_{on}
0	Turn on S_1 and S_2 if t< t_{on} Turn off all the switches when t>t_{on}

Under normal operating conditions, the fourth leg is used to balance the NP voltage. In order to achieve this goal, the locally averaged current over a modulation period injected by the fourth leg into the NP $(\bar{i}_L)$ should be equal to

$$\begin{aligned} \bar{i}_L &= \bar{i}_{\mathrm{NP}} + \bar{i}_{\mathrm{com}}, \\ \bar{i}_{\mathrm{com}} &= 2C\frac{v_{C2} - \frac{V_{\mathrm{dc}}}{2}}{T_s} \\ \bar{i}_{\mathrm{NP}} &= d_a\bar{i}_a + d_b\bar{i}_b + d_c\bar{i}_c \end{aligned} \tag{1}$$

where $\bar{i}_{\mathrm{NP}}$ is the locally averaged value of the NP current injected by the three main legs of the converter over a switching period, d_x is the normalized duty cycle during which phase x (for $x = \{a, b, c\}$) is connected to the NP, $\bar{i}_x$ is the locally averaged current of phase x during a switching period, $\bar{i}_{\mathrm{com}}$ is the current necessary to compensate for possible imbalances of the voltages on the capacitors, and T_s is the sample or switching period.

In order to inject this locally averaged current into the NP, the fourth leg should be switched as indicated in Table I. In this table, it is assumed that "1" means true and "0" means false.

The switching time t_{on} can be calculated in each modulation period by means of the following expression:

$$t_{\mathrm{on}} = \sqrt{\frac{2LT_s\,|\bar{i}_L|}{V_{\mathrm{dc}}}} \tag{2}$$

where V_{dc} is the dc-link voltage and L is the value of the inductance connected to the fourth leg.