

Design and Tuning of a Modified Power-Based PLL for Single-Phase Grid-Connected Power Conditioning Systems

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Abstract—One of the most important aspects for the proper operation of the single-phase grid-tied power-conditioning systems is the synchronization with the utility grid. Among various synchronization techniques, phase locked loop (PLL)-based algorithms have found a lot of interest for the advantages they present. Typically, the single-phase PLLs use a sinusoidal multiplier as the phase detector (PD). These PLLs are generally referred to as the power-based PLL (pPLL). In this paper, the drawbacks associated with the pPLL technique (i.e., the sensitivity to the grid voltage variations, and the double-frequency oscillations that appear in the estimated phase/frequency) are discussed in detail, and some of the previously reported solutions are examined. Then, to overcome these drawbacks, a simple and effective technique, called the double-frequency and amplitude compensation (DFAC) method is proposed. The effectiveness of the proposed method is evaluated through a detailed mathematical analysis. A systematic design method to fine-tune the PLL parameters is then suggested, which guarantees a fast transient response, a high disturbance rejection capability, and a robust performance. Finally, the simulation and experimental results are presented, which highlight the effectiveness of the proposed PLL.

Index Terms—Frequency estimation, phase estimation, phase-locked loop (PLL), power-based PLL (pPLL), single phase grid-connected converters, synchronization.

I. INTRODUCTION

THE phase-angle and frequency of the utility grid are vital information for most single-phase grid-tied power-conditioning systems, such as active power filters [1], dynamic voltage restorers [2], [3], flexible ac transmission systems

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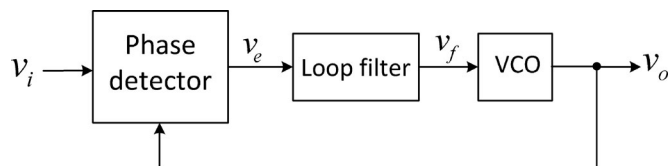


Fig. 1. Basic scheme of a single-phase PLL.

(FACTS) [4]–[6], uninterruptible power supplies (UPS) [7], and distributed power generation and storage systems [8].

To estimate the frequency and phase-angle of the single-phase signals various methods have been proposed in the literature [4]–[25]. Among these techniques, the phase locked loop (PLL)-based algorithms are the most widely accepted ones, due to their simplicity, robustness, and effectiveness [4]–[20]. Focusing on grid-connected power converter applications, a PLL is a closed-loop feedback control system, which synchronizes its output signal in frequency, as well as in phase, with the grid voltage fundamental component. In spite of their differences, all PLL techniques are composed of three basic parts, namely: 1) phase detector (PD), 2) loop filter (LF), and 3) voltage-controlled oscillator, as illustrated in Fig. 1.

The main difference among different PLLs usually lies in how the PD block is implemented. Typically, the single-phase PLLs use a sinusoidal multiplier as the PD. These PLLs are generally referred to as the power-based PLL (pPLL). In the following section, the drawbacks associated with the pPLL technique (i.e., the sensitivity to the grid voltage variations, and the double-frequency oscillations that appear in the estimated phase/frequency) are discussed in detail, and some of the previously reported solutions are examined. Then, to overcome these drawbacks, a simple and effective technique, called the double-frequency and amplitude compensation (DFAC) method is proposed. Through a detailed mathematical analysis it is shown that the proposed DFAC method successfully compensates for the undesired double-frequency oscillations, as well as the input voltage amplitude variations, while keeping a fast dynamic response and robust performance for the PLL. It is worth remarking that, for three-phase PLLs, tackling the generation of the low-order oscillations in the estimated phase/frequency has been well addressed [26], [27].

An accurate tuning of the PLL parameters requires considering several factors such as the stability margin, the disturbance rejection ability, and the transient response to the phase-jump and frequency variation. Some suggestions to design the PLL

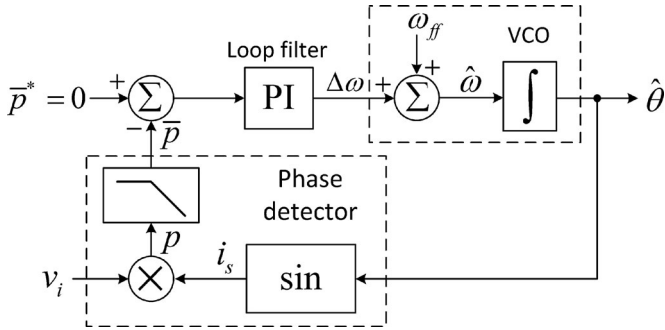


Fig. 2. Single-phase pPLL.

parameters have been presented in the literature [7], [10]–[13], [28], [29]. In this paper, a systematic design procedure to fine-tune the PLL parameters is proposed. The suggested approach guarantees a fast transient response, a high disturbance rejection capability, and a robust performance.

This paper is organized as follows. Section II provides a brief review of the pPLL topology. The main drawbacks of the pPLL, and previously reported solutions are also discussed in this section. The proposed PD is presented in Section III. The small-signal modeling of the proposed PLL, here, referred to as DFAC-pPLL, and the stability analysis are addressed in Section IV. The proposed systematic design method is discussed in Section V. The simulation and experimental results are presented in Section VI. Finally, Section VII concludes this paper.

II. BACKGROUND

The basic scheme of the single-phase pPLL is depicted in Fig. 2 [7]. Throughout this section and the following section, for the sake of simplicity, the input voltage v_i is assumed to be a pure sine wave, i.e. $v_i = V \cos \theta$, where V and $\theta (= \omega t + \phi)$ are the input voltage amplitude and angle, respectively. ω_{ff} is the nominal value of the frequency ω , and ϕ is the phase-angle. The superscript “ $\hat{\cdot}$ ” denotes the estimated quantities.

The pPLL, as seen, uses a sinusoidal multiplier followed by a low-pass filter (LPF) for the PD. Note that the PD block tries to emulate an active power calculation unit. If the PD block output signal (i.e., \bar{p}) is zero, then the input voltage v_i and the fictitious current i_s will be in quadrature relative to each other [7]. In this case, the estimated value of the voltage angle $\hat{\theta}$ is equal to the real value θ .

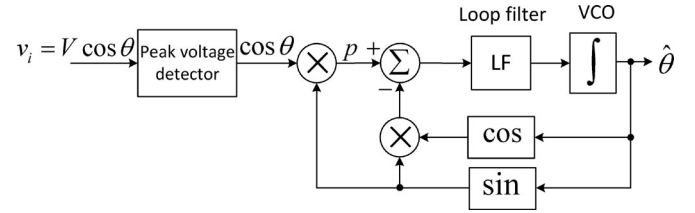
Based on Fig. 2, the fictitious power p can be expressed as

$$p = v_i i_s = V \cos \theta \sin \hat{\theta}. \quad (1)$$

Applying the product-to-sum trigonometric identity, yields

$$p = \underbrace{\frac{V}{2} \sin(\hat{\theta} - \theta)}_{\text{determ}} + \underbrace{\frac{V}{2} \sin(\hat{\theta} + \theta)}_{\text{double-frequency term}}. \quad (2)$$

Supposing a small difference between θ and $\hat{\theta}$, (2) can be divided into two parts: a small dc term that has the information on the phase difference, and a high-amplitude double-frequency

Fig. 3. Proposed PLL by Thacker *et al.* [12].

disturbance term that must be filtered out to keep up the phase jittering within an acceptable range [30].

To cancel out the undesired double-frequency component from the fictitious power p , one can use either a first- (or second-) order LPF with a low cutoff frequency or a high-order LPF with a higher cutoff frequency. In addition to stability problems, using a high-order LPF imposes a high computational load on the control system [31]. On the other hand, using a low-order LPF with a low cutoff frequency, significantly degrades the transient performance of the PLL. Another approach is to use a notch filter tuned at twice the input voltage fundamental frequency. Because of the grid frequency variations, the notch filter should be adaptive, which increases the system cost and complexity.

Some improvements to the pPLL have been suggested in [16], [17]. In these techniques, referred to as orthogonal signal generation (OSG)-based techniques, the fundamental component of the input voltage is shifted by 90° to generate a fictitious phase signal, thus making it possible to represent the single-phase system as a pseudo two-phase ($\alpha\beta$) system. Applying the well-known park ($\alpha\beta \rightarrow dq$) transformation to the two phase ($\alpha\beta$) system, yields the phase error information without generating the undesired double-frequency component. It should be noticed that the main difference among different OSG-based techniques lies in how the fictitious orthogonal signal is generated. In spite of their differences, all OSG-based techniques suffer from some common drawbacks, such as high sensitivity to the grid frequency variations, and relatively high complexity [18].

The most recent improvement to the pPLL is that proposed by Thacker *et al.* [12]. In their method, a unity value for the input voltage amplitude is assumed that is realized by a peak voltage detection (PVD) scheme at the input of the PLL. Under this assumption, and in phase/frequency-locked conditions (i.e., $\theta \cong \hat{\theta}$), the unwanted double-frequency component is filtered out by subtracting a product term (i.e., $\sin \hat{\theta} \cos \hat{\theta}$) from the fictitious power p , as shown in Fig. 3. Although this PLL exhibits some improvements over the pPLL technique, it suffers from a major drawback; regardless of the cost and the complexity imposed by the PVD, the exact and fast estimation of the input voltage amplitude may not always be possible. In this case, the PLL performance is significantly degraded.

The dependence of the PLL stability and dynamic performance on the input voltage amplitude is other drawback of the pPLL. It is shown that the voltage amplitude V contributes as a gain in the forward path of the PLL small-signal model [32]. Thus, under the voltage sag condition, which is commonly associated with the phase-angle jump [33], [34], the PLL transient

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